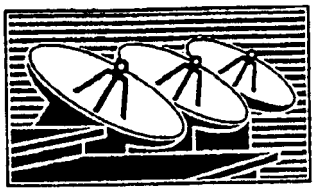

530—STGT—IE311

OPERATION AND MAINTENANCE MANUAL

INTEGRATED RECEIVER

April 1992

NASA
National Aeronautics and Space Administration

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

OPERATION AND MAINTENANCE MANUAL

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PART NUMBER 7472100 (INTERSTATE ELECTRONICS)

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DCN CONTROL SHEET

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Section 1 — General Description

1–1 Introduction

1–1.1 This Level 1 manual is limited to unit operation and maintenance in the installed condition while in the local (maintenance) control mode. Also included is the information necessary to replace and maintain the chassis and all applicable line replaceable units (LRUs) for the Integrated Receiver (IR), part number 7472100.

1–1.2 The IR provides data recovery and tracking data for all S-Band Single Access (SSA), S-Band Shuttle (SSHR), and Multiple Access (MA) return user services. For K-Band Single Access (KSA) return user services, the IR provides tracking data for all services, including K-Band Shuttle return services (KSHR). The IR provides autotrack error signal detection for all KSA services, except KSHR Mode 2. The IR provides data recovery for all Low Data Rate KSA return services.

1–1.3 The IR provides the following essential functions, as required, when applicable:

a. Provide Doppler correction, including the capability to:

   (1) Receive Doppler updates (ephemeris data) from the data bus.

   (2) Maintain a Forward Model of the Doppler compensation and control performed on the forward link.

b. Despread and track the received PN spread signal.

c. Recover PN code epoch and clock and perform range measurements and time transfer measurements. For MA services, provide PN code and lock status as output signals.

d. Demodulate the carrier.

e. Recover carrier and perform Doppler measurement, including the S-Shuttle case where the return signal is carrier only (no modulation). This includes all User Services Subsystem (USS) return services except KSHR Mode 2 (frequency modulation mode).

f. Recover symbol clock and detect symbols, including single and dual channel configurations for all USS return services, except KSA high data rate.

g. Support data delay measurement.

h. Perform ground terminal delay measurement for Range Zero Set.

i. Resolve data channel and phase ambiguity.

j. Provide deinterleaving and convolutional decoding, including SSHR unique rate 1/3 decoding. Provide the capability to bypass the decoders.

k. Provide format conversion of recovered symbols and data so that the output data stream is non-return to zero-level (NRZ-L).

l. Provide as outputs the recovered data streams with synchronous data clocks, with the following exceptions:

   (1) Clamp the data output (in-phase (I) and quadrature (Q) independently) to a logical-1 when there is detected loss of data in the channel.

   (2) During times when a data channel is clamped to a logical-1 due to a loss of data in the channel, maintain the data clock output signal.

m. For KSA return services, including KSHR Mode 1, provide carrier recovery for Doppler measurements and perform autotrack error signal detection. Autotrack error signal detection is not available for KSHR Mode 2 (frequency modulation mode).

n. For KSHR Mode 1 (quadrature double sideband mode), perform extraction, acquisition, and demodulation of the subcarrier from the 370-MHz IF input. For KSHR Mode 2, provide data and carrier recovery on the Shuttle

subcarrier provided to the unit on the 8.5-MHz IF input.

o. For SSA return services, including SSHR, provide SSA combining.

p. Generate status data, including self-test and fault isolation information. Provide required status data (including Eb/No measurement, channel error rates, and channel lock times) to both the front panel and to the data bus. Additional status data may be provided to the data bus that is not available on the front panel.

q. Communicate with the primary interface via a MIL-STD-1553B data bus. Table 1-1 lists the various command and report names and fields used to communicate over the 1553 bus.

r. Support maintenance and operation, provide front panel and maintenance panel controls, indicators, and test points.

1–1.4 The information in this manual is presented in seven sections: Section 1, General Description; Section 2, Installation; Section 3, Operation; Section 4, Theory of Operation; Section 5, Maintenance; Section 6, Parts list; and Section 7, Drawings.

1–1.5 Section 1 describes the use, capabilities, and technical specifications of the IR. The IR (see figure 1-1 ; shown with top cover removed) is an integral part of the Second Tracking and Data Relay Satellite System (TDRSS) Ground Terminal (STGT) Return USS.

1–1.6 This OP-06-1 manual was prepared for the National Aeronautics and Space Administration (NASA) by GE Contract No. NAS5-33000.

1–2 Physical Description

For the purposes of this manual, the major components described are those that are maintained, replaced, or repaired in the installed condition (Level 1 LRUs). Refer to table 1-2 for a listing of the major components of the IR and the illustrations in section 6 for their location. The following information describes the physical characteristics of the chassis and LRUs:

a. Chassis Assembly (IR): EMI-designed to be housed in a module shell or standard 19-inch NASA rack. Its physical characteristics are: 12.22 +0.00/-0.03 inches in height, 17.75 inches maximum chassis width (including slides), 24 inches maximum depth, 18.97 +0.00/-0.03 panel width, with a total weight more than 74 pounds and not to exceed 85 pounds. The IR makes use of VME double-height printed wiring assemblies (PWAs), RF modules with front panel SMB coaxial, DIN 41612 type M connectors, modular power supplies, and a common baseplate allowing for all internal PWA and RF module (non-RF) interfaces.

b. Power Supply No. 1 (PS1): 4.875” x 7.75” x 12.25” screw-mounted, terminal board wire connections, fan-cooled, 12 pounds maximum, LAMBDA LFQ series power supply.

c. Power Supply No. 2 (PS2): 2.5” x 4.9” x 14.0” screw-mounted, terminal board wire connections, 5.5 pounds maximum, convection-cooled multi-output power supply.

d. Modem Control Processor (MCP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, front panel mounted LEDs and switches for status/control, and dual front panel mounted RS-232/RS-422/RS- 485 interface selectable (9-pin) connectors. Utilizes four plug-in sockets to house the latest MCP/Exec firmware release IC chip set (4); SP7472100-xxx (J21, J23, J25, and J27), where xxx represents the release version. Refer to the label on the inside of the unit top cover for applicable release version.

e. Acquisition Processor (ACQR) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a 40-pin DIN 41612 test point connector.

f. PN Processor (PNP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a 40-pin DIN 41612 test point connector.

Table 1—1. IR Commands and Reports

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
SET STATE	Start checkword Initialization type Initialization data End checkword	CONFIG - URATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds KSA Eb/No disable Service type Mode DG1 or SSHR Setup miscellaneous parameters I/Q power ratio I data format Q data format I encoding Q encoding I symbol format Q symbol format Operational light Single/dual channel modulation I data rate Q data rate Feedback taps Initialize A register value Initialize C register value SSA combining delay I symbol jitter Q symbol jitter Return IF offset frequency KSAR I channel data recovery KSAR Q channel data recovery STGT return translation frequency TDRS return translation frequency Service maximum I data rate Service maximum Q data rate End checkword
SPECIFIC CONFIG - URATION	Start checkword KSA Eb/No disable Configuration item bit map Service type Service mode Setup miscellaneous parameters I/Q power ratio I data format Q data format I encoding Q encoding I symbol format Q symbol format Operational light Single/dual channel modulation I data rate Q data rate Feedback taps Initialize A register value Initialize C register value SSA combining delay I symbol jitter Q symbol jitter Return IF offset frequency KSAR I channel data recovery KSAR Q channel data recovery STGT return translation frequency TDRS return translation frequency Service maximum I data rate Service maximum Q data rate End checkword		

Table 1—1. IR Commands and Reports (Continued)

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
COMMON CONFIG - URATION	Start checkword Bit map Forward IF offset frequency Forward translation frequency Forward Doppler configuration End checkword	COMMON CONFIG - URATION	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Forward IF offset frequency Forward translation frequency Forward Doppler configuration End checkword
BURN ALERT	Start checkword Transition to powered flight Uncertainty time End checkword		
EXPAND FREQUENCY SEARCH	Start checkword End checkword	TRACKING	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Lock status Range delay 1 second average Doppler frequency Return 1st epoch measurement Return 2nd epoch measurement Time bias estimate End checkword
START ACQUISITION	Start checkword End checkword		
ZERO DOPPLER	Start checkword Effective time; hours Effective time; minutes Effective time; seconds CMD LOL End checkword		
FORWARD FREQUENCY SWEEP	Start checkword Effective time; hours Effective time; minutes Effective time; seconds End checkword	PERFORM - ANCE	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds Lock status Commands not executed map Commands not accepted map Commands not executed error code Commands not accepted error code Operating state
FORWARD DOPPLER COMPEN - SATION CONTROL	Start checkword Effective time; hours Effective time; minutes Effective time; seconds Command word Duration Target delta frequency Return to profile End checkword		
START FORWARD MODEL	Start checkword Effective time; hours Effective time; minutes Effective time; seconds End checkword		

Table 1—1. IR Commands and Reports (Continued)

COMMAND	FIELD DEFINITION	REPORT	FIELD DEFINITION
FORWARD BREAKLOCK	Start checkword Effective time; hours Effective time; minutes Effective time; seconds Duration Step size End checkword	PERFORM - ANCE (continued)	I coherent data AGC status Q coherent data AGC status 370 IF AGC status 8.5 IF AGC status Ephemeris status Forward model status Receiver control status Eb/No - I channel Eb/No - Q channel I symbol error count Q symbol error count I channel lock time Q channel lock time Confidence test status Online BIT status Local/remote status HRDC Present IND End checkword
COLD START	Start checkword Effective time; hours Effective time; minutes Effective time; seconds Snapshot time; hours Snapshot time; minutes Snapshot time; seconds PN code state IF carrier frequency Carrier/Doppler compensation status Sweep bias state End checkword	EXTENDED BIT	Start checkword Report time; day Report time; hours Report time; minutes Report time; seconds MCP test results VME test results TIME test results DMDP test results Demod ASIC I test results Demod ASIC Q test results Signal level test PNP test results Correlator test results End checkword

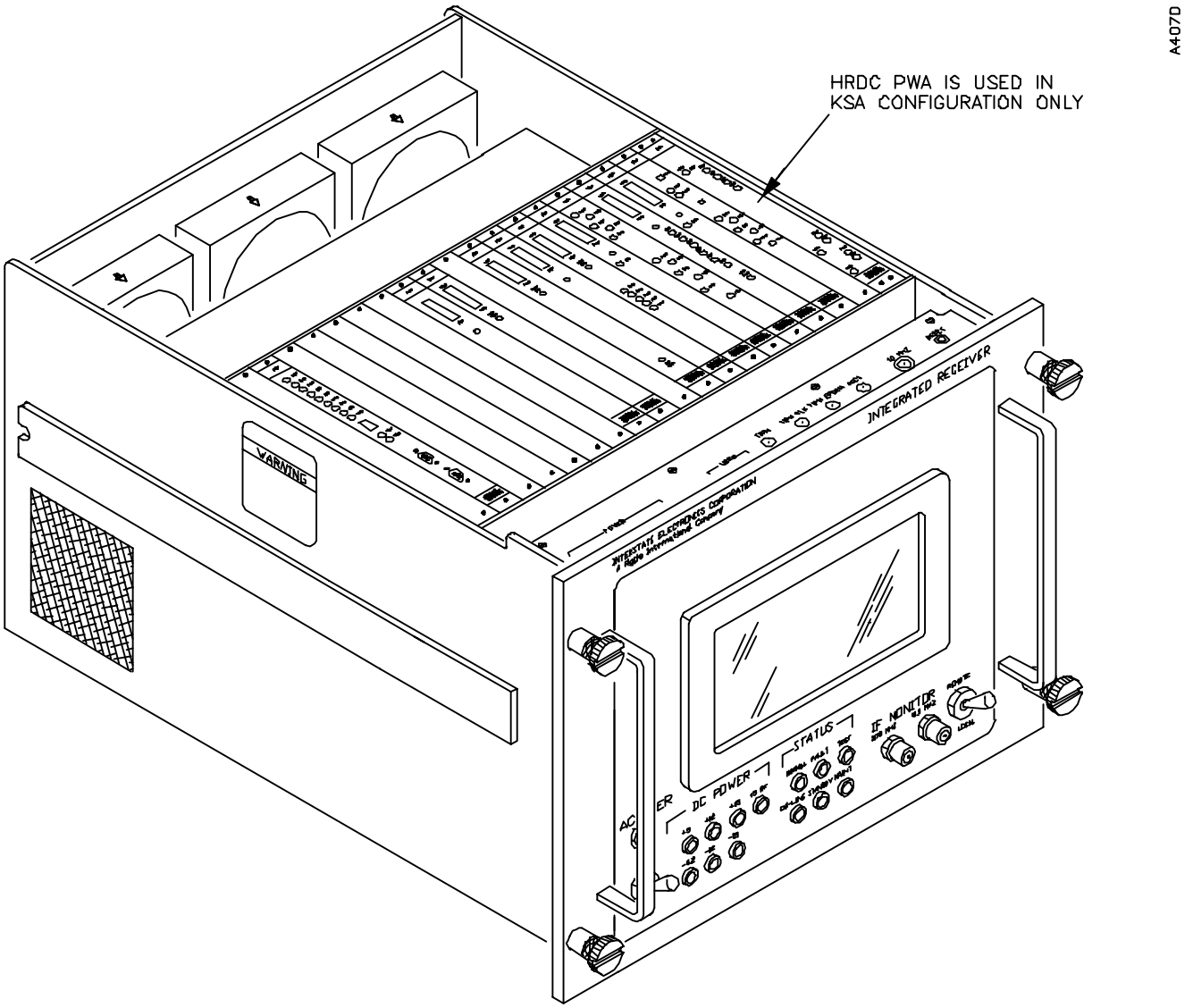


Figure 1—1. Integrated Receiver
P/N 7472100

g. Timing Generator (TIME) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, front-panel-mounted dual SMB coaxial connectors, and a 40-pin DIN 41612 test point connector.

h. Demod Processor (DMDP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, and a 40-pin DIN 41612 test point connector. Utilizes two plug-in sockets to house the latest DMDP firmware release IC chip set (2); SP7472110-xxx (J11 and J12), where xxx represents the release version. Refer to the label on the inside of the unit top cover for applicable release version.

i. Output Processor (OUTP) PWA: 9.2” x 6.3” printed wiring assembly, screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, front panel mounted LEDs, and a 40-pin DIN 41612 test point connector.

j. Demod Symbol Synchronizer (DMSS I/Q) PWA: 9.2” x 6.3” printed wiring assembly,

Table 1—2. Major Components

COMPONENT	REF. DES.	FIG. NO.
Integrated Receiver		1 - 1
Power Supply No. 1	1A2	6 - 3 - 4
Power Supply No. 2	1A3	6 - 3 - 3
Modem Control Processor PWA	1A4A1	6 - 1 - 7
Acquisition Processor PWA	1A4A7	6 - 1 - 6
PN Processor PWA	1A4A8	6 - 1 - 5
Timing Generator PWA	1A4A10	6 - 1 - 4
Demodulator Processor PWA	1A4A11	6 - 1 - 3
Output Processor PWA	1A4A12	6 - 1 - 2
Demodulator Symbol Synchronizer PWA (Q)	1A4A13	6 - 1 - 8
RF Downconverter 2 PWA	1A4A14	6 - 1 - 9
Synthesizer PWA	1A4A15	6 - 1 - 10
Demodulator Symbol Synchronizer PWA (I)	1A4A16	6 - 1 - 11
RF Downconverter 1 PWA	1A4A17	6 - 1 - 12
High Rate Downconverter PWA (KSA configurations only)	1A4A18	6 - 1 - 13
Power Supply No. 3	1A5	6 - 3 - 2
Touch Panel Display	1A7A1	6 - 2 - 7

screw-mounted, VME double-height, dual 96-pin DIN 41612 connectors, a front-panel-mounted SMB coaxial connector, and a 40-pin DIN 41612 test point connector.

k. RF Downconverter No. 2 (RFDC2) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each and front-panel SMB coaxial connectors (twelve).

l. Synthesizer (SYNTH) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each, front-panel-mounted LED, front-panel mounted SMB coaxial connectors (seven), and a 40- pin DIN 41612 test point connector.

m. RF Downconverter No. 1 (RFDC1) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each and front-panel SMB coaxial connectors (nine).

n. High-Rate Downconverter (HRDC) PWA: 9.2" x 6.3" printed wiring assembly, screw-mounted, VME double-height, dual 60-pin DIN 41612 type M connectors with four RF connectors each and front-panel SMB coaxial connectors (eleven). Used in KSA configurations only.

o. Touch Panel Display: 9.0" x 12.5" x 3.74" interactive alphanumeric display with an Amp Mate- N-Lok 1-480270-0 power connector, a 3M 3399-6040 parallel input connector, a 3M 3399- 6026 parallel output connector, and a 25-pin male D-type serial connector.

p. Power supply No. 3 (PS3): 4.9" x 4.03" x 2.78" screw-mounted, hard-wire connections, 12 pounds maximum, 130.0 Vdc power supply.

1–3 Functional Description

This paragraph provides a brief functional description of the chassis and each Level 1 LRU. Items covered include the functions of the chassis as a whole and then each LRU as it applies to pertinent input/output signals.

1–3.1 IR Chassis Assembly

The IR is used interchangeably in the KSA low data rate (LDR) equipment, SSA equipment, or MA receiver/transmit equipment. The IR interfaces with the SSA, KSA, and MA control hardware configuration items (HWCIs) and common time and frequency system (CTFS) in the SSA, KSA, and MA portions of the return USS equipment groups, respectively. Furthermore, the IR interfaces with the MA beamforming equipment HWCI in the MA portion of the return service USS. Figure 1-2 shows the SSA interface configuration, figure 1-3 shows the KSA low data rate interface configuration, and figure 1-4 shows the MA receive/transmit interface configuration. Refer to figure 4-1 for the functional block diagram.

1–3.2 Power Supply No. 1

PS1 accepts the 120-Vac site-supplied power and outputs regulated +5.0 Vdc, +5.0 RF Vdc, and +/-15.0 Vdc source power for circuits throughout the IR.

1–3.3 Power Supply No. 2

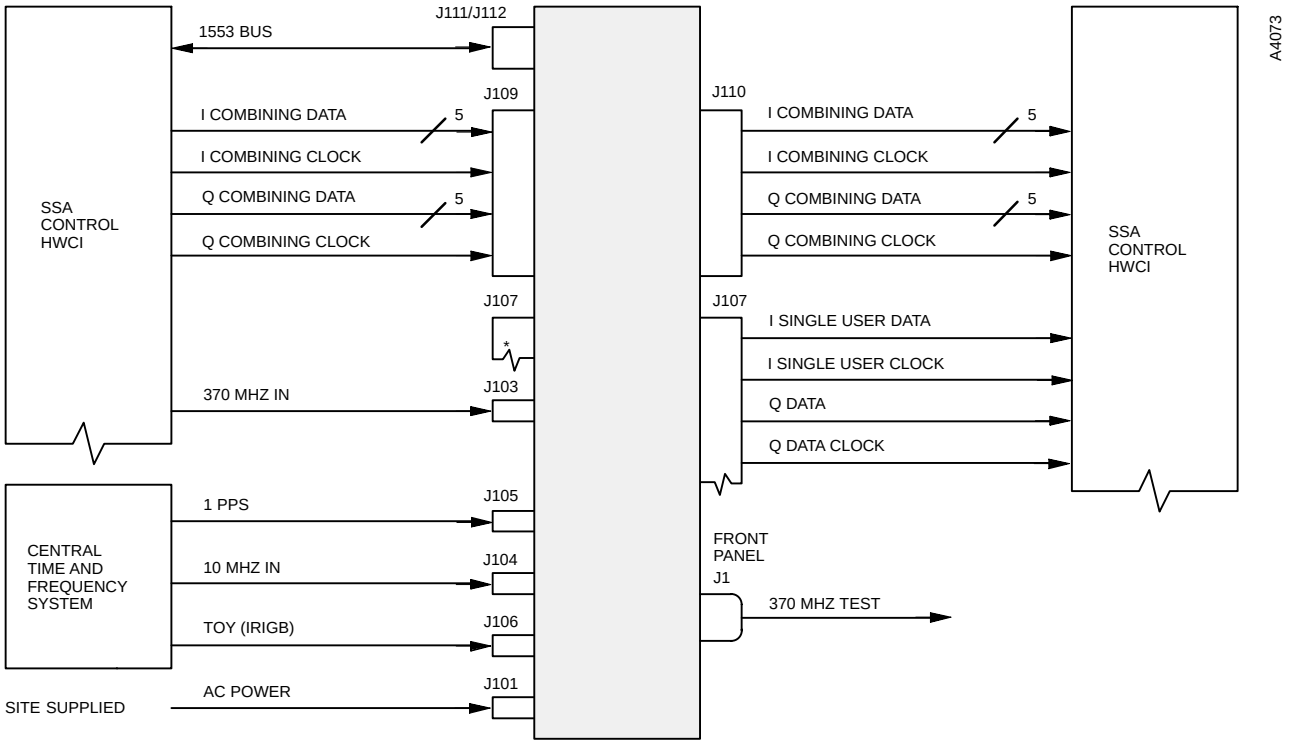
PS2 accepts the 120-Vac site-supplied power and outputs regulated -5.2 Vdc and +/-12.0 Vdc source power for circuits throughout the IR.

1–3.4 Power Supply No. 3

PS3 accepts the 120-Vac site-supplied power and outputs regulated +130.0 Vdc to the touch panel display.

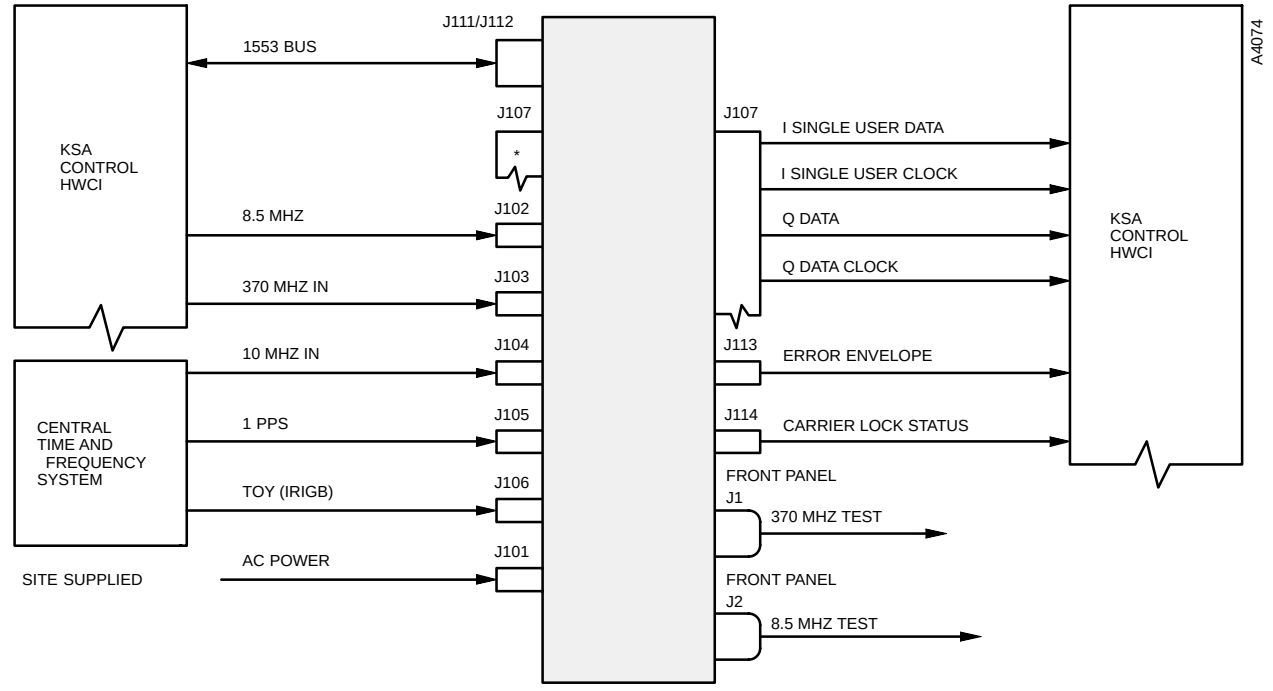
1–3.5 Modem Control Processor PWA

1–3.5.1 MCP Functions – The MCP provides the required computations, scheduling of events,



* REMOTE TERMINAL ADDRESS IS JUMPERED WITHIN THE SITE INTERFACING CONNECTOR.

Figure 1—2. Integrated Receiver Interfaces for SSA Equipment Configuration



* REMOTE TERMINAL ADDRESS IS JUMPERED WITHIN THE SITE INTERFACING CONNECTOR.

Figure 1—3. Integrated Receiver Interfaces for KSA Low Data Rate Equipment Configuration

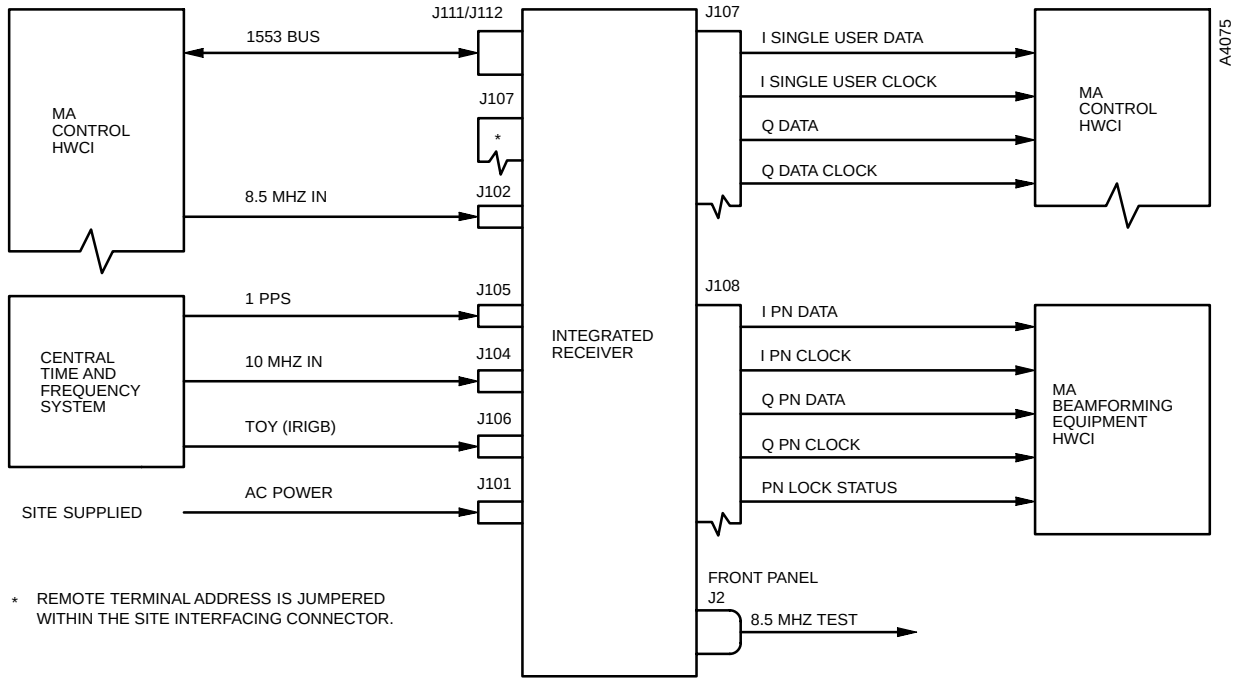


Figure 1–4. Integrated Receiver Interfaces for MA Receiver/Transmit Equipment Configuration

and overall control of the IR operations via the VMEbus. The MCP provides the following:

a. A 68030 central processing unit (CPU) and 68882 floating-point coprocessor, both operating at 25 MHz.

b. Capability of up to 5 mega-instructions per second (MIPS) through the 1-Mbyte onboard static random access memory (SRAM) and the on-chip cache.

c. Two 68561 multiprotocol communications controllers (MPCCs) for serial I/O (RS-232 compatible interface with one channel-selectable RS-232/RS-422/RS-485).

d. Two parallel interface and timer (PI/T) devices for local control, interrupt level control, and timer functions.

e. Two 68153 bus interrupter modules (BIMs) for all local interrupts.

1–3.5.2 MCP Interfaces – The MCP interfaces with the following:

a. PNP (via VMEbus) to provide pseudorandom noise (PN) acquisition control, tracking, and PN NCO control.

b. TIME (via VMEbus) to provide control of the 1553 IR interface, IRIG-B data, NCO, and accept various timing and epoch interrupts.

c. Front panel to control the interactive touch-panel display.

d. ACQR (via VMEbus) to provide configuration/operation control and accept peak search detect data.

e. DMDP (via VMEbus) to provide configuration/operation control and accept status data.

1–3.6 Acquisition Processor PWA

1–3.6.1 ACQR Functions – The ACQR processes the output of either one or both channels of I and Q acquisition correlator data produced by

the DMSSs. After data from each DMSS is accumulated (coherent combine), the two channels of data may be added together (coherent channel combine). The magnitude of each bin is calculated, may be added to that of the other channel (noncoherent channel combine), and is accumulated (noncoherent combine). A peak value and index are found, and an interrupt is generated to indicate completion of the accumulation interval. The number of coherent and noncoherent combines is controlled by the PNP and the operating mode is selected by the MCP via the VMEbus.

1–3.6.2 ACQR Interfaces – The ACQR interfaces with the following:

a. DMSSs to accept I and Q correlator data.

b. PNP to accept timing and control signals. These signals direct the data flow through the ACQR, particularly the number of coherent and noncoherent combines intervals and/or subintervals.

c. MCP (via the VMEbus) to accept configuration/operation control data and provide peak detect data.

1–3.7 PN Processor PWA

1–3.7.1 PNP Functions – The PNP generates PN replica codes compatible with TDRSS services. It contains two generators that produce I and Q code strings (one for acquisition and one for tracking purposes). It produces the required clocks and control signals for PN acquisition and tracking. The acquisition code generator provides for step search and acquisition accumulator control. The tracking code generator provides I and Q early, ontime, and late replica code strings.

1–3.7.2 PNP Interfaces – The PNP interfaces with the following:

a. DMSSs to provide PN data and associated clocks.

b. ACQR to provide timing and control signals. These signals direct the data flow through the ACQR, particularly the number of coherent and noncoherent combines intervals and/or subintervals.

c. MCP (via the VMEbus) to accept configuration/operation control data.

d. TIME to accept timing signals and output PN code epochs.

1–3.8 Timing Generator PWA

1–3.8.1 TIME Functions – The TIME provides the following functions: time - of - year (TOY) data from IRIGB, timing and epoch interrupts, time transfer measurement (epoch count), communicates with the VMEbus via a MIL - STD - 1553 interface, control/status interface between RF PWAs and VMEbus, two variable numerically controlled oscillators (NCOs), power source measurements, and front panel interface.

1–3.8.2 TIME Interfaces – The TIME interfaces with the following:

a. Time - of - year (seconds, minutes, hours, and days) information to the VMEbus from the input serial IRIG - B data.

b. A controlled 1553 interface with the VMEbus.

c. PNP to provide timing signals and accept PN code epochs.

d. Control/status communication between the RF modules, TIME, and the VMEbus.

e. Timing and epoch interrupts to the VMEbus from the 1 PPS, epoch, and 50 - MHz signals and accept masking of any or all of these interrupts. An epoch count to the VMEbus. The epoch count is defined as the number of 10 - MHz clocks between the 1 PPS and the epoch mark.

f. An NCO output to SYNTH which is VMEbus controlled.

g. Output digital voltage measurements of various analog signals and power sources to the VMEbus upon command.

h. A register that is capable of being observed at test points on the P3 connector and is controllable by the VMEbus. A driver register

that interfaces the VMEbus and P2 connector.

i. DMSSs and DMDP to provide various timing signals.

1–3.9 Demodulator Processor PWA

1–3.9.1 DMDP Functions – The DMDP consists of a digital signal processor (DSP), a fast fourier transform (FFT) controller, and the associated hardware to perform the following functions:

a. Communicate control, configuration, and status information with the MCP via the VMEbus.

b. Control signal tracking loops as required by the configuration. This function uses an FFT process to acquire the carrier, and second- and third-order digital phase-lock loops (PLLs) to track it. Control information is sent to, and status and data received from the DMSSs via the TMS bus.

c. Provide non-coherent automatic gain control (AGC) and dc-bias compensation to maintain proper signal input levels from the RF section of the unit to the digital processing section.

d. Send control information to the OUTP (via the TMS bus) to direct the decoding and autotrack functions.

1–3.9.2 DMDP Interfaces – DMDP interfaces with the following:

a. DMSSs to provide signal tracking loop control (via TMS bus) and accept FFT I/Q data.

b. OUTP (via TMS bus) to provide control information for the decoding and autotrack functions.

c. MCP (via the VMEbus) to accept configuration/operation control data and provide status data.

d. RFDCs to provide AGC and I/Q offset control.

1–3.10 Output Processor PWA

1–3.10.1 OUTP Functions – The OUTP provides the following functions:

a. Accept control information from and output status data to the DMDP via the TMS bus.

b. Provide deinterleaving and decovering of interleaved I and Q symbol data.

c. Provide Viterbi decoding of I and Q symbol data.

d. Provide Shuttle decoding of the I symbol data.

e. Provide SSA combining and synchronization of the I and Q symbol data with input baseband demodulated I and Q signals from a second co-located IR. Also provide baseband I and Q signals to a second co-located IR for SSA combining purposes.

f. Provide the KSA Autotrack error envelope function.

g. Differentially drive input PNP timing, lock and status signals.

h. Differentially decode NRZ-M and NRZ-S formatted I and Q symbol data to NRZ-L formatted data.

i. Provide five LEDs representing the lock status of the OUTP data processing configuration.

1–3.10.2 OUTP Interfaces – OUTP interfaces with the following:

a. DMDP to accept (via TMS bus) control information for the decoding and autotrack functions along with a carrier lock status signal.

b. DMSSs to accept symbol data and associated clock.

c. PNP to accept I/Q acquisition code stream, status, and clock.

d. External interface to supply the selected TDRSS return service data and status information.

1–3.11 Demod Symbol Synchronizer PWA

1–3.11.1 DMSS Functions – The DMSS consists of two digital finite impulse response (FIR) filters, an application specific integrated circuit (ASIC) referred to as the Demod chip, two 2 - bit fast acquisition correlators referred to as Comcor2 chips, and associated hardware. The DMSS performs the following functions:

a. Provides matched digital FIR filtering for the I and Q digital inputs.

b. The Demod chip provides integrate - and - dump matched filtering, timing error detection, phase error detection, timing loop filtering, PN acquisition and tracking, and PN early/late error detection functions. The numerically controlled oscillator (NCO) in the Demod chip provides the main clock that is used to generate all other clocks required for the chip.

c. Capable of processing either the digitized baseband signal inputs from the RF downconverters or FIR filter inputs from the other DMSS.

d. Provides PN code acquisition function using two 2 - bit, multi - tap, flexible correlators. The correlator's length is selected by software and can be from 4 to 1024 taps. The NCO in the Demod chip is used to provide the 8.5 - MHz carrier frequency acquisition function.

e. Provide 5 - bit differential I and Q symbol data for output to the OUTP.

f. Provides all the required clocks such as sample, symbol, and bit - rate clocks and output them to be used elsewhere in the unit. Communicates control, status, and data with the DMDP via the TMS bus.

1–3.11.2 DMSS Interfaces – DMSS interfaces with the following:

a. DMDP for a controlled TMS bus interface and FFT I/Q data.

b. SYNTH to accept a 70 - MHz clock for Demod chip NCO.

c. RFDCs to accept digitized I, Q, and BB (RFDC2 only) components of the processed return service IF signal and provide an 8.5 - MHz LO signal and sample clock for proper downconversion and digitization.

d. TIME to accept various timing signals.

e. PNP to accept PN data and associated clocks.

f. ACQR to provide I and Q correlator data.

g. Other DMSS to provide and accept FIR filtered/combine data and clocks.

h. OUTP to provide symbol data and associated clock.

1–3.12 RF Downconverter No. 2

1–3.12.1 RFDC2 Functions – During certain SSA and KSA configurations, RFDC2 is used to process a 370 - MHz IF input and downconvert it to 70 MHz using the 300 - MHz LO input. The 70 - MHz IF is split, with one side output to RFDC1 and the other side is quadrature downconverted and digitized to produce 8 - bit I and Q components for output. During high - rate KSA configurations, RFDC2 outputs the 370 - MHz IF signal to the HRDC and then accepts the high - rate I and Q baseband signals from the HRDC. The high - rate I and Q baseband signals are digitized and output instead of the RFDC baseband processed signals.

1–3.12.2 RFDC2 Interfaces – RFDC2 interfaces with the following:

a. DMSS (Q) to provide digitized I_i and Q_i components of the processed low - rate return service or digitized Q BB components from the high - rate downconverter (HRDC). Also, accept an 8.5 - MHz LO (Q) signal and sample clock for proper downconversion and digitization.

b. SYNTH to acquire the 300 - MHz LO and 61.5 - MHz LO downconversion signals and a 70 - MHz test signal.

c. RFDC1 to acquire and provide the 70 - MHz IF and to output I/Q baseband component signals in MA mode only.

d. TIME to accept control signals for bandwidth mode and self test selection.

e. HRDC to accept I/Q BB and BB inputs and output the 300-MHz LO and 61.5-MHz LO downconversion signals.

f. DMDP for I, Q, BB, offset, non-coherent AGC, and +10 vdc reference.

1–3.13 Synthesizer PWA

1–3.13.1 SYNTH Functions – The SYNTH uses PLLs and divider circuits to generate the necessary clocks and timing signals needed by the IR circuits. The SYNTH uses the 10 - MHz input from the system CTFS to ensure system phase synchronization. The SYNTH also provides an LED indicating the 61.5 - MHz PLL is locked, the 140 - MHz PLL is locked, and the 10 - MHz reference signal is present.

1–3.13.2 SYNTH Interfaces – SYNTH interfaces with the following:

a. RFDC1 to provide the 61.5-MHz LO downconversion signal and an 8.5-MHz test signal.

b. RFDC2 to provide the 300-MHz LO and 61.5-MHz LO downconversion signals and a 70-MHz test signal.

c. HRDC to provide the 300-MHz LO downconversion signal.

d. TIME to provide 50-MHz clock and PLL status signals and accept a 20-MHz/ 8.5-MHz (depending upon configuration) base timing signal. Also, SYNTH accepts an MA select signal for output signal selection.

e. DMSS (I) and (Q) to provide a 70-MHz clock for Demod chip NCO.

1–3.14 RF Downconverter No. 1

1–3.14.1 RFDC1 Functions – RFDC1 is used to process two different signal inputs, depending on the return service configuration. During certain KSA and MA configurations, it processes an 8.5 - MHz IF input with a 61.5 - MHz LO signal to generate a 70 - MHz IF that is downconverted and digitized to produce 8 - bit I and Q components. During certain SSA and KSA configurations, it processes a 70 - MHz IF, (from RF downconverter 2), that is downconverted and digitized to produce 8 - bit I and Q components. RFDC1 can also accept I and Q baseband signals for digitization and output versus processing the 70 - MHz IF signal.

1–3.14.2 RFDC1 Interfaces – RFDC1 interfaces with the following:

a. DMSS (I) to provide digitized I_i and Q_i, components of the processed return service IF signal and accept an 8.5-MHz LO (I) signal and sample clock for proper downconversion and digitization.

b. SYNTH to acquire the 61.5-MHz LO downconversion signal and an 8.5-MHz test input.

c. RFDC2 to acquire and provide 70-MHz IF and I/Q baseband component signals.

d. TIME to accept control and output AGC status.

e. DMDP for I, Q offset.

1–3.15 High–Rate Downconverter

1–3.15.1 HRDC Functions – The HRDC accepts a modulated 370 - MHz signal and converts it to baseband. During high - rate KSA configurations, RFDC2 outputs the 370 - MHz IF signal to the HRDC and then accepts the high - rate I and Q baseband signals from the HRDC. The high - rate I and Q baseband signals are digitized and output instead of the RFDC baseband processed signals.

1–3.15.2 HRDC Interfaces – HRDC interfaces with the following:

a. SW3 (subcarrier switch) and SW4 (370-MHz switch) for signal selection processing.

b. TIME to accept control signals for signal processing selection.

c. RFDC2 to provide I/Q BB and detected BB outputs and input the 70-MHz LO downconversion signals.

d. Synthesizer for 300 MHz LO.

1–3.16 Touch Panel Display

The touch panel display is an interactive terminal using the Argus alphanumeric display module to display messages and a touch-input infrared switch matrix to record user responses. The Argus alphanumeric display uses dc-excited plasma technology to display characters in a 5x7 dot format with underline and forward cursor capability. The switch matrix is an X-Y array of active locations formed by intersecting beams of infrared light generated by LED elements. When a set of X-Y beams is broken, a switch closure is detected and the switch position is transmitted to the MCP. Each active area (approximately 0.2x0.2 inches) is centrally located between two horizontal display character locations. Thus, there are 240 active switch locations arranged in 12 rows of 20 columns.

1–4 Condensed Data

As applicable, refer to the following tables for IR Level 1 maintenance:

a. Table 1-3, Electrical Characteristics; this table lists all input/output electrical characteristics of the IR chassis and Level 1 LRUs.

b. Table 1-4, NASA Drawings; this table lists all IR chassis and Level 1 LRU technical illustrations contained in sections 1 and 5 that have NASA drawing numbers assigned.

c. Table 1-5, Environmental Requirements; this table lists environmental conditions that the IR will not suffer permanent degradation or damage when subjected to.

d. Table 1-6, Equipment Required, but Not Supplied; this table lists all equipment required for IR Level 1 maintenance, but not supplied with the unit.

e. Table 1-7, Consumables; this table lists all required consumables for IR Level 1 maintenance.

1–5 Special Tools and Test Equipment

Table 1-8 lists and describes the special tools and test equipment required to maintain the IR while in the installed condition (Level 1 maintenance). All chassis-installed maintenance is performed using standard handtools. If any of the listed items are not available, equivalent part numbers may be used. The IR is supported, as part of the Return USS, by the performance measuring and monitoring (PMMS) test equipment (PTE) and the maintenance test group (MTG). The PTE provides for preservice, post-maintenance, and end-to-end test (EET) verification of the IR and associated equipment. MTG provides control of test configuration, injection of test stimuli, measurements of equipment responses to stimuli, and display results in a manner to permit failure localization.

Table 1—3. Electrical Characteristics

PARAMETER	DESCRIPTION
PHYSICAL CHARACTERISTICS	
Panel height	12.22, +0.00/ - 0.03 inches
Panel width	18.97, +0.00/ - 0.03 inches
Chassis depth	24 inches, maximum
Chassis width	17.75 inches, maximum (including slides)
Weight	85 pounds, maximum
POWER REQUIREMENTS	
Voltage	120 Vac; +/ - 10% voltage regulation, single phase
Frequency	60 +/ - 3 Hz
Transients	+/ - 15% of nominal voltage; surge for less than 0.5 second
Power consumption	700 watts, maximum
Panel connectors	Rear panel: 1A1J101, AC connector
370 - MHz INPUT IF/TEST POINT	
Nominal frequency	370 MHz
Reference bandwidth	Refer to signal plus noise power parameter
Nominal Impedance	50 ohms
Signal plus noise level in the reference bandwidth	Input signal plus noise power at the 370 MHz IF varies according to service and according to whether the input originates from a user return signal or from the PMMS.
SSAR	The input power at the 370 MHz IF input will be - 25.5 dBm, +/ - 6 dB, in the following reference 3 dB bandwidths centered about 370 MHz: User return signal The reference 3 dB bandwidth for an SSA user return signal, or for an end - to - end PMMS signal is 17 MHz. Internal loopback The reference 3 dB bandwidth for an SSA PMMS internal loopback test signal is 30 MHz. Spurious signals Regardless of signal source, the total RSS value of all spurious signals within a 17 MHz bandwidth, centered about 370 MHz, will be - 30 dBc, maximum; no single spurious signal will exceed - 40 dBc.

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
370 - MHz INPUT IF/TEST POINT (Continued)	
KSAR	The input power at the 370 MHz IF input will be - 20.0 dBm, +/ - 4 dB, in the following reference 3 dB bandwidths centered about 370 MHz: User return signal The reference 3 dB bandwidth for a KSA user return signal, or for an end - to - end PMMS signal is 240 MHz. Internal loopback, Test Modem The reference 3 dB bandwidth for a KSA PMMS internal loopback signal which has noise added by the KSA LDR equipment Test Modem is 30 MHz. Internal loopback, HDR PTE The reference 3 dB bandwidth for a KSA PMMS internal loopback signal which has noise added by the KSA HDR equipment is 300 MHz. Spurious signals Regardless of signal source, the total RSS value of all spurious signals over a 30 MHz bandwidth, centered about 370 MHz, will be - 30 dBc, maximum. Individual spurious signals from 10 MHz to 2,000 MHz will be - 40 dBc, maximum.
Input VSWR	Better than 1.3:1 over the reference bandwidth
Panel connectors	Rear panel; 1A1J103, SMA female
8.5 - MHz INPUT IF	
Nominal Frequency	8.5 MHz
Reference Bandwidth	Refer to signal plus noise power parameter
Nominal Impedance	50 ohms
Signal plus noise level in the reference bandwidth	
KSAR	The input power at the 8.5 MHz IF input will be - 20.0 dBm, +/ - 4 dB, in a reference 3 dB 15 MHz low pass band. No distinction is made between user signals and test signals.
MAR	The input power at the 8.5 MHz IF input will be - 20 dBm in the following referenced bandwidths:

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
370 - MHz INPUT IF/TEST POINT (Continued)	
MAR (Continued)	User return signal The reference 3 dB bandwidth for an MA user return signal, or for an end - to - end PMMS signal is 6 MHz, centered about 8.5 MHz. Signal plus noise may vary by plus or minus 20 dB in this bandwidth. Internal loopback The reference 3 dB bandwidth for an MA PMMS internal loopback signal is a 15 MHz low pass. Signal plus noise may vary by plus or minus 4 dB in this bandwidth. Spurious signals Regardless of signal source, the total spurious power within the 6 MHz reference band is - 30 dBc, maxi mum. Individual spurious signals from 1 MHz to 16 MHz will be - 40 dBc, maximum.
Input VSWR	Better than 1.3:1 over a 6 MHz bandwidth centered about 8.5 MHz
Panel connectors	Rear panel; 1A1J102, SMA female
SSA COMBINING SIGNALS	
Data rate	100 bps to 3 Mbps on I and Q
Clock Frequency	Equal to data rate and synchronous with data
Levels	RS - 422A
Data type	Complementary balanced differential TTL
Input impedance	100 ohms +/ - 2 % line - to - line for the combining inputs
Output impedance	Less than 10 ohms for the combining outputs
Panel connectors	Rear panel; 1A1J109, 37 - pin male D type, 1A1J110, 37 - pin female D type

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
CTFS INPUTS	
10 MHz	
Frequency	10 MHz
Waveform	Sinusoidal
Impedance	50 ohms
Level	+11 dBm +/ - 2 dB into 50 ohms
Single Sideband Phase Noise	Better than - 140 dBc for 1 kHz offset measured in a 1 Hz bandwidth
Accuracy	+/ - 4 x 10^{-12}
Stability	+/ - 8.5 x 10^{-13} long term (100 seconds) +/ - 5 x 10 short term (1 second)
Input VSWR	Better than 1.3:1 in a bandwidth from 9.5 MHz to 10.5 MHz
Panel connectors	Rear panel: 1A1J104, SMA female
1 PPS	
Frequency	1 Hz
Waveform	Single ended, rectangular pulse
Impedance	50 ohms
Level	TTL levels
Pulse Width, t	100 microseconds, +/ - 0.1%
Rise and Fall Times	< 10 nanoseconds
Jitter	< 2 nanoseconds
Accuracy	< +/ - 25 nanoseconds referenced to the CTFS master epoch
Panel connectors	Rear panel: 1A1J105, SMA female
Time of Year (TOY)	
Signal Format	IRIG - B level shift
Impedance	50 ohms, nominal
Levels	TTL into 50 ohms
Panel connectors	Rear panel: 1A1J106, SMA female

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
1553 BUS	
Description	MIL - STD - 1553B Digital Time Division Command Response Multiplex Data Bus with the IR configured as a remote terminal. Refer to ICD STGT - HE - 06 - 2; GES - STGT - 0004 for interface configuration and control information.
Mode	Single channel, redundant
Coupling	Transformer coupled
Remote terminal address	See table 4 - 1, jumpered on connector J107
Parity	Odd
Panel connectors	Rear panel: 1A1J111, 1A1J112 Twinax (threaded)
OUTPUT I/Q DATA AND CLOCK SIGNALS	
Signals	I Data/Single User Data I Clock/Single User Clock Q Data Q Clock
Data Rate	100 bps to 6 Mbps on I and Q, 100 bps to 12 Mbps on I for a single channel user
Clock Rate	Equal to data rate and synchronous with data
Type/Level	Complimentary balance differential TTL
Output impedance	Less than 10 ohms
Panel connectors	Rear panel: 1A1J107, 25 - pin female D type
PN DATA AND CLOCK SIGNALS	
Signals	I PN Data Q PN Data PN Lock Status
PN Chip Rate	3.08 Mcps, nominal
PN Clock Rate	Equal to chip rate and synchronous with PN data
Absolute Delay	1265 nanoseconds
Variation in Delay	Less than 30 nanoseconds over 24 hours
PN Code Status	Logic 0 = Code Lock Logic 1 = No Code Lock (Lock is referenced to the I channel)
Type/Level	Complimentary balance differential TTL; RS - 422A
Panel connectors	Rear panel: 1A1J108, 15 - pin female D type

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
AUTOTRACK ERROR ENVELOPE	
Level	12 volts differential, maximum
Bandwidth	Analog
Impedance matching	Differential twisted pair with nominal 249 ohm terminations to ground at the receiver
Panel connectors	Rear panel: 1A1J113, Twinax, 3 lug
CARRIER LOOP STATUS	
Level	Logic 1 = Carrier Locked Logic 0 = Carrier Not Locked
Type/level	Logic is complimentary balanced differential TTL; RS - 422A
Panel connectors	Rear panel: 1A1J114, Twinax, 3 - lug
ACQUISITION PROCESSOR PWA	
Power Consumption	17.5 watts, typical; 23.6 watts, maximum
Input Power	+5.00 +/ - 0.25 Vdc; 3.5 amperes, typical; 4.5 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
DEMOD SYMBOL SYNCHRONIZER PWA	
Power Consumption	30 watts, maximum
Input Power	+5.00 +/ - 0.25 Vdc; 5.5 amperes, maximum - 5.2 +/ - 0.25 Vdc; 0.2 ampere, maximum +15.0 +/ - 0.25 Vdc; 0.1 ampere, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
RF DOWN CONVERTER NO. 1	
Power Consumption	20.3 watts, maximum
Input Power	+5.00 +/ - 0.25 Vdc; 0.8 amperes, maximum - 5.2 +/ - 0.25 Vdc; 0.4 ampere, maximum +15.0 +/ - 0.5 Vdc; 0.7 ampere, maximum - 15.0 +/ - 0.5 Vdc; 0.2 ampere, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc ECL Logic 0: - 1.105 to - 0.8 Vdc ECL Logic 1: - 1.950 to - 1.475 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
RF DOWN CONVERTER NO. 2	
Power Consumption	20 watts, maximum
Input Power	+5.00 +/ - 0.25 Vdc; 0.8 amperes, maximum - 5.2 +/ - 0.25 Vdc; 0.4 ampere, maximum +15.0 +/ - 0.5 Vdc; 0.7 ampere, maximum - 15.0 +/ - 0.5 Vdc; 0.2 ampere, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc ECL Logic 0: - 1.105 to - 0.8 Vdc ECL Logic 1: - 1.950 to - 1.475 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
TIMING GENERATOR PWA	
Power Consumption	43 watts, maximum; 33 watts, typical
Input Power	+5.00 +/ - 0.25 Vdc; 5.4 amperes, maximum; 5.0 amperes, typical - 5.2 +/ - 0.25 Vdc; 1.5 amperes, maximum; 0.75 amperes, typical +12.0 +/ - 1.2 Vdc; 1 milliampere, maximum; 1 microampere, typical - 12.0 +/ - 1.2 Vdc; 1 milliampere, maximum; 1 microampere, typical +15.0 +/ - 1.5 Vdc; 0.2 amperes, maximum; 0.1 amperes, typical - 15.0 +/ - 1.5 Vdc; 0.2 amperes, maximum; 0.1 amperes, typical

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
TIMING GENERATOR PWA (Continued)	
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc ECL Logic 0: - 1.5 to - 1.9 Vdc ECL Logic 1: - 0.6 to - 1.3 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum 1553: 20 volts p - p, maximum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc ECL Logic 0: - 1.5 to - 1.9 Vdc ECL Logic 1: - 0.6 to - 1.3 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum 1553: per MIL - STD - 1553
RF Outputs	Frequencies of 8.5 +/ - 0.25 MHz and 20 +/ - 1.6 MHz with a 50 ohm nominal impedance and at +/ - 2 dBm
SYNTHESIZER PWA	
Power Consumption	37 watts, maximum
Input Power	+5.00 +/ - 0.25 Vdc; 0.75 amperes, maximum - 5.2 +/ - 0.25 Vdc; 0.75 amperes, maximum +15.0 +/ - 0.5 Vdc; 1.75 amperes, maximum - 15.0 +/ - 0.5 Vdc; 0.2 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc ECL Logic 0: - 1.85 to - 1.63 Vdc ECL Logic 1: - 0.98 to - 0.81 Vdc
PN PROCESSOR PWA	
Power Consumption	24.2 watts, maximum; 17.8 watts, typical
Input Power	+5.00 +/ - 0.25 Vdc; 4.0 amperes, maximum; 3.0 amperes, typical - 5.2 +/ - 0.25 Vdc; 0.7 amperes, maximum; 0.48 amperes, typical +12.0 +/ - 0.25 Vdc; 19 milliamperes, maximum; 8 milliamperes, typical - 12.0 +/ - 0.25 Vdc; 25 milliamperes, maximum; 16 milliamperes, typical

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
PN PROCESSOR PWA (Continued)	
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	ECL: 1 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
DEMOD PROCESSOR PWA	
Power Consumption	21.0 watts, maximum; 15.0 watts, typical
Input Power	+5.00 +/ - 0.25 Vdc; 4.0 amperes, maximum; 3.0 amperes, typical +15.0 +/ - 1.5 Vdc; 30 milliamperes, maximum; 20 milliamperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.6 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
OUTPUT PROCESSOR PWA	
Power Consumption	30 watts, maximum; 25 watts, typical
Input Power	+5.00 +/ - 0.25 Vdc; 5.8 amperes, maximum; 4.9 amperes, typical +15.0 +/ - 1.5 Vdc; 55 milliamperes, maximum; 25 milliamperes, typical - 15.0 +/ - 1.5 Vdc; 55 milliamperes, maximum; 25 milliamperes, typical
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Differential Inputs	TTL: 0.7 Vdc, minimum ECL: 0.7 Vdc, minimum
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
Differential Outputs	TTL: 2.0 Vdc, minimum ECL: 0.8 Vdc, minimum

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
HIGH - RATE DOWN CONVERTER PWA	
Power Consumption	27.1 watts, maximum; 26.2 watts, typical
Input Power	+5.00 +/ - 0.25 Vdc; 0.7 amperes, maximum - 5.20 +/ - 0.25 Vdc; 0.6 amperes, maximum +15.0 +/ - 0.5 Vdc; 1.0 amperes, maximum - 15.0 +/ - 0.5 Vdc; 0.3 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc
POWER SUPPLY NO. 1	
AC Input	95 - 132 Vac at 47 - 440 Hz; Input power at maximum output power 633 watts
Efficiency	75% minimum at maximum output power
Inrush Limiting	75 amperes maximum
EMI Suppression	FCC Docket 20780, Class A and VDE 0871, Class A
Output Voltage	+5.00 +/ - 0.25 Vdc, adjustable; 75, 66, and 57 amperes maximum at 72, 90, and 108 degrees Fahrenheit respectively; Minimum preload of 19.0 amperes is required on +5 Vdc output for maximum current on auxiliary outputs +15.00 Vdc +/ - 0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit respectively - 15.00 Vdc +/ - 0.5 Vdc, adjustable; 7.2, 6.4, and 5.5 amperes maximum at 72, 90, and 108 degrees Fahrenheit respectively +5.00 (RF) +/ - 0.25 Vdc, adjustable; 7.5, 6.7, and 6.0 amperes maximum at 72, 90, and 108 degrees Fahrenheit respectively
Output Power	475, 420, and 362 watts maximum at 72, 90, and 108 degrees Fahrenheit respectively
POWER SUPPLY NO. 2	
AC Input	90 - 132 Vac at 47 - 63 Hz
Efficiency	65% to 75%
Inrush Limiting	65 amperes maximum peak with electronic soft - start (150 amperes on 220 watts)

Table 1—3. Electrical Characteristics (Continued)

PARAMETER	DESCRIPTION
POWER SUPPLY NO. 2 (Continued)	
EMI Suppression	FCC Docket 20780, Class A and VDE 0871, Class A
Output Voltage	- 5.2 +/ - 0.25 Vdc, adjustable; 30.0 amperes, maximum; 25 amperes, typical
	+12.00 +/ - 0.25 Vdc, adjustable; 5.0 amperes, maximum; 4.0 amperes, typical
	- 12.00 +/ - 0.25 Vdc, adjustable; 6.0 amperes, maximum; 3.0 amperes, typical
POWER SUPPLY NO. 3	
AC Input	104 - 126 Vac at 50 - 60 Hz; 0.75 amperes at 115 Vac, maximum
Output Voltage	+130 Vdc at 0.18 amperes, maximum
Output Regulation	2%
TOUCH PANEL DISPLAY	
Panel Supply Voltage	+150 Vdc, maximum; +120 to +130 Vdc, nominal
Panel Current	160 milliamperes, +/ - 25%
Positive Logic Supply Voltage	+7.0 Vdc, maximum; 4.75 to 5.25 Vdc, nominal
Logic Current	2.0 amperes, +/ - 25%
High Level Logic (Data)	+7.0 Vdc, maximum; 2.4 to 5.5, nominal
Low Level Logic (Data)	- 1.5 Vdc, maximum; - 0.5 to 0.8 Vdc, nominal
High Level RS - 232 - C	+15.0 Vdc, maximum; 3 to 15 Vdc, nominal
Low Level RS - 232 - C	- 15.0 Vdc, maximum; - 3 to - 15 Vdc, nominal
MODEM CONTROL PROCESSOR PWA	
Power Consumption	34 watts, maximum
Input Power	+5.00 +/ - 0.25 Vdc; 5.7 amperes, maximum +12.0 +/ - 0.25 Vdc; 0.2 amperes, maximum - 12.0 +/ - 0.25 Vdc; 0.2 amperes, maximum
Logic Inputs	TTL Logic 0: 0.0 to 0.8 Vdc TTL Logic 1: 2.0 to 5.0 Vdc
Logic Outputs	TTL Logic 0: 0.0 to 0.5 Vdc TTL Logic 1: 2.4 to 5.0 Vdc

Table 1—4. NASA Drawings		
DRAWING NO.	DESCRIPTION	PAGE
Not applicable.		

Table 1—5. Environmental Requirements	
PARAMETER	DESCRIPTION
OPERATING ENVIRONMENT	
Temperature	+50 to +100 degrees Fahrenheit
Temperature rate	Temperature rate of change shall not exceed 10 degrees per hour
Humidity	From 20 to 80 percent without condensation
Altitude	Sea level to 12,000 feet
NONOPERATING ENVIRONMENT	
Temperature	-20 to +160 degrees Fahrenheit for periods of at least 4 days
Humidity	From 0 to 100 percent relative humidity, noncondensing environment
Altitude	Sea level to 35,000 feet
Solar radiation	350 BTU/ft@/hour

Table 1—6. Equipment Required, but Not Supplied		
MFR. MODEL./PART NO.	DESCRIPTION	FUNCTION
Not applicable.		

Table 1—7. Consumables			
NOMENCLATURE	SPECIFICATION NUMBER/NSN	PART NO./ CAGE	APPLICATION
Not applicable.			

Table 1—8. Special Tools and Test Equipment

RECOMMENDED MODEL/PART NO.	MANUFACTURER (FSCM/CAGE)	COMMON NAME	USE	FIG. NO.
5120 - 00 - 278 - 1267	81348	No. 1 flat - tipped screw - driver	Remove top cover	N/A
5120 - 01 - 022 - 9953	55719	No. 1 cross - tipped screw - driver	Remove/replace PWAs	N/A
6625 - 01 - 235 - 2911	89356	Multimeter	Measure voltages/ resistances	N/A
6966 - C	78976	Gun, heat	Heat shrink - wrap	N/A
Commercial source		Vacuum cleaner	Clean unit interior	N/A
Commercial source		Snub - nosed pliers	Remove/replace lampholder, switch	N/A
Commercial source		IC chip puller	Remove/replace MCP and DMDP IC chips	N/A
499 - 920 - 012	07421	Wirecutters/strippers	Remove/replace lampholder	N/A
499 - 925 - 014	07421	Soldering iron	Remove/replace lampholder	N/A
HP 5345A	Hewlett - Packard	Universal Counter	Measure frequency of RF signals	N/A

Section 2 — Installation

2—1 Introduction

This section contains chassis unpacking, installation, removal, packaging, and storage/shipment information for the Integrated Receiver in the STGT. This section also includes a detailed view of the rear panel and associated connectors, figure 2-1. Refer to table 4-1 for connector pin identification information.

2—2 Chassis Installation in STGT

The IR is a complete unit and requires no internal wiring, strapping, or cable changes other than factory setup. The unit is designed to be housed in the return service KSA low data rate equipment HWCI cabinet, SSA equipment HWCI cabinet, or MA receiver/transmit equipment HWCI cabinet; the rack numbers are: 1007, 1008, 1009, 1010, 1011, 1013, 1014, 1016, 1025, 1028, 1110, 1111, 1122. All external cable and wiring interfaces are site supplied.

2—3 Unpacking

The IR is shipped as a complete unit with all subassemblies (PWAs, power supplies, etc.) installed. The unit is wrapped in antistatic bubble-wrap material and placed in a shipping container as shown in figure 2-2. To unpack the unit, proceed as follows:

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

NOTE

Before unpacking the unit, inspect the shipping container for signs of external damage. If the container is damaged, notify the carrier as well as the authorized field service personnel.

Keep the shipping container for future use, storage, or shipment for service/repair. Refer to the repackaging for shipment and storage paragraphs later in this section.

a. With the shipping container on the floor, topside up, open the shipping container by carefully cutting the plastic packing tape.

b. Remove the polyethylene packing material to gain access to the unit.

c. Remove the unit wrapped in antistatic bubble-wrap material. Remove the bubble-wrap from around the unit and place unit on floor (or other acceptable work area surface), topside up.

d. Perform a general inspection inventory of the major components (see table 1-2) to ensure the unit is complete.

2—4 Chassis Installation

WARNING

The IR requires three people to safely lift and place/remove the unit into/from the cabinet assembly. Also, removing or installing items of equipment while the equipment cabinet is energized could result in damage to equipment or injury to personnel. Ensure that all power is removed from the equipment rack before attempting assembly.

The following procedure applies to all configurational uses of the IR.

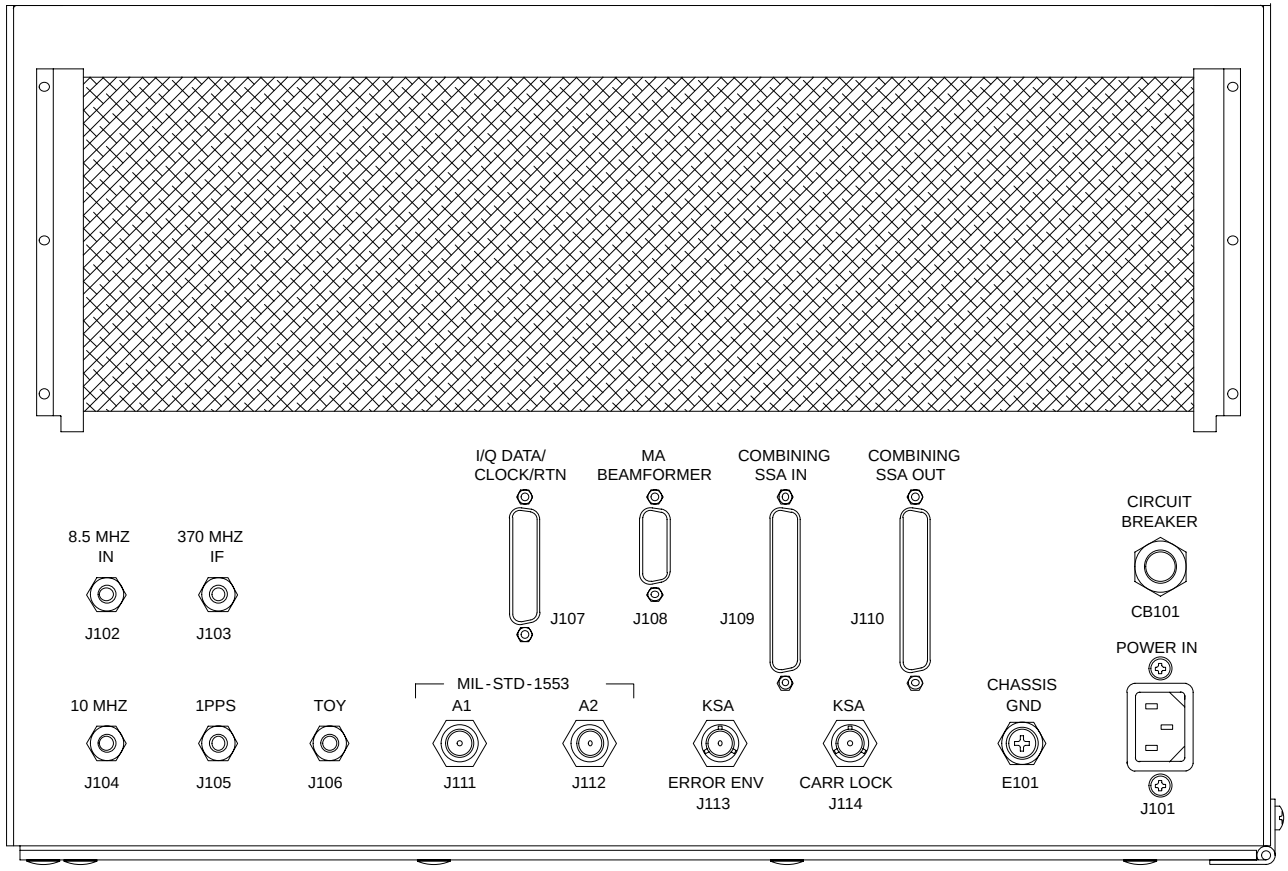


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Figure 2—1. Integrated Receiver Rear Panel

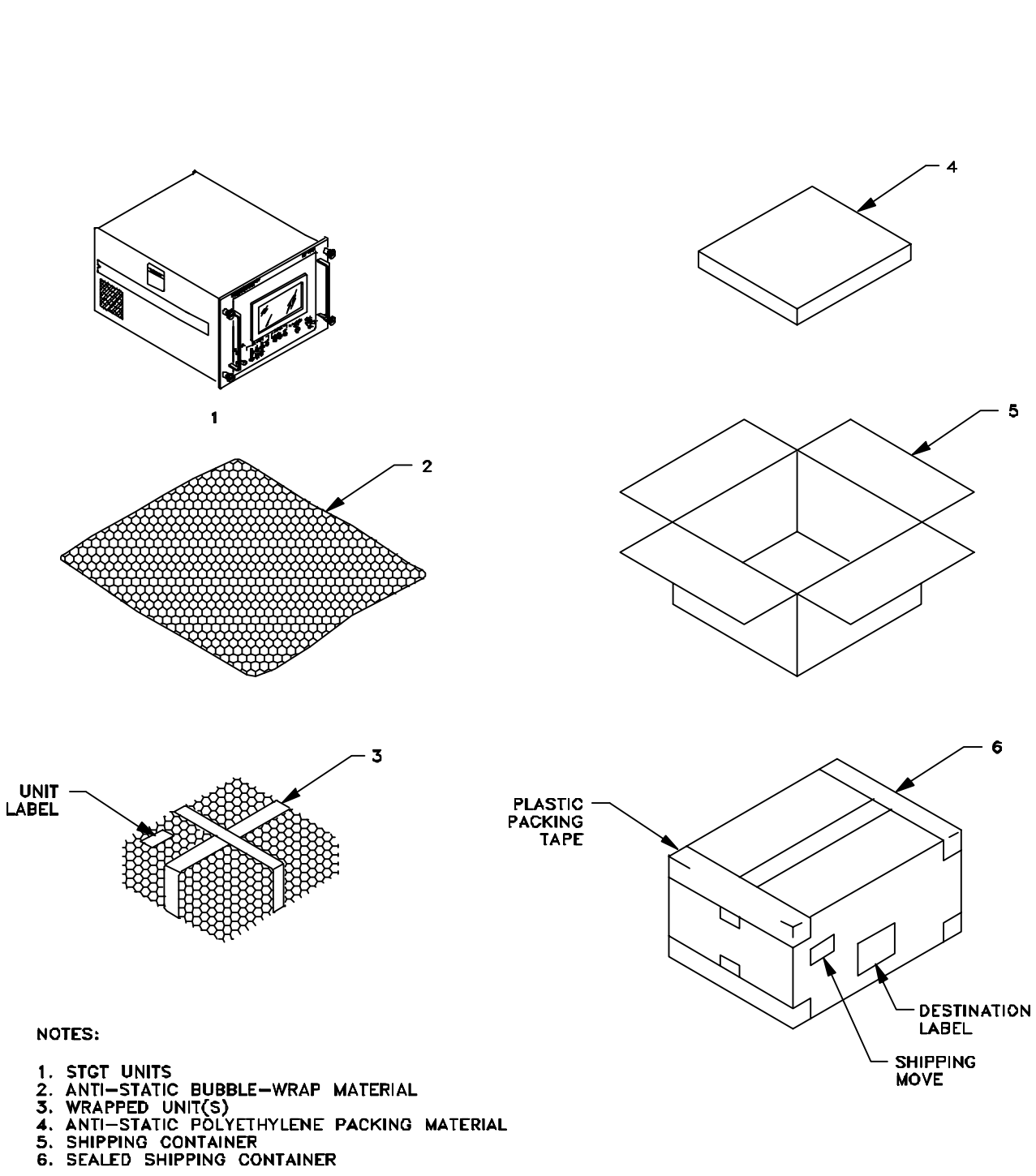

Figure 2—2. Equipment Packing/Unpacking

a. Remove all electrical power from the equipment cabinet where the unit is to be installed.

b. Gain access to the rear of the equipment cabinet assembly and ensure all cabling is clear for installation of unit.

c. Extend cabinet section rail guides until guide lock seats.

d. Raise the unit (three people required), with each person placing one hand on front panel handle and the other hand placed underneath the unit; guide the unit section slide rails into their respective cabinet rail guides until the quick lock/disconnect mechanism locks into position.

e. Disengage the rail guide locks and slide unit slowly into equipment cabinet to ensure a clear entry.

f. At rear of cabinet, attach all applicable cable connectors (use finger force on all SMA connectors) and grounding straps to unit. Refer to figures 1-2, 1-3, or 1-4 and applicable site cable interfacing documentation, depending upon applicable configuration.

g. At the front of the unit, use a flat-tipped (common) screwdriver to tighten the four front-panel captive screws to the cabinet assembly.

h. Make a visual inspection to ensure that no cables are being pinched and that the unit is properly seated within the cabinet assembly.

i. Apply power to the cabinet assembly and all cabinet assembly units.

j. Perform the turn-on and self-check procedures found in section 3 to verify proper unit operation.

2—5 Chassis Removal

WARNING

The IR requires three people to safely lift and place/remove the unit into/ from the cabinet assembly. Also, removing or installing items of equipment while the equipment cabinet is energized could result in damage to equipment or injury to personnel. Ensure that all power is removed from the equipment rack before attempting disassembly.

The following procedure describes the steps necessary to remove the IR from the equipment cabinet. Proceed as follows:

a. Perform the shutdown procedure found in section 3.

b. Remove all electrical power from the equipment cabinet.

c. Loosen the four captive screws holding the unit in the cabinet.

d. Gain access to the rear of the equipment cabinet assembly. Ensure that cables are properly tagged. Disconnect all cables and ground straps attached to the unit. Connect the 10-MHz cable to a 50 ohm dummy load.

e. Slide the unit forward until the rail guide locks are set to the locked position.

f. On each side of the unit, press the rail guide quick lock/disconnect mechanism and pull the unit forward just past the point where the mechanism locks. With three people, one on each side and one in front of the unit, each person placing one hand on front panel handle and the other hand underneath the unit, slide the unit out of the cabinet rail guides and place the unit on a workbench.

g. At the equipment cabinet, disengage the rail guide locks and slide the rail guides back into the cabinet.

2—6 Unit Packaging

The following procedure provides the necessary instructions to package the IR for storage or shipment. Refer to figure 2-2.

a. Obtain a quantity of antistatic bubble-wrap material (Federal Specification PPP-C-795, class 2) sufficient to wrap the unit to a thickness of at least 3-1/2 inches. Material must be of 1/2-inch thickness, and multiple wrappings must add up to a minimum of 3-1/2 inches.

b. Wrap unit with bubble-wrap and secure with masking tape.

c. Fill out a unit container label per STDN No. 507, Network Logistics Manual which includes the following information:

   (1) National stock number or activity control number

   (2) Part number

   (3) Part name

   (4) Serial number

   (5) Manufacturer's name

   (6) Quantity

d. Secure the label to the wrapped unit.

e. Place the maintenance report (when applicable) in an envelope. Identify on the envelope that it contains the maintenance report and attach the envelope to the unit.

f. Place unit in a cushioned shipping/storage container. The shipping/storage container should be in accordance with customer logistics procedures.

g. Place sufficient antistatic polyethylene packing material (type I) around the unit to ensure no movement during shipment.

h. Seal the container with plastic packing tape or other suitably strong tape.

i. Fill out a shipping label per STDN No. 507, Network Logistics Manual.

j. Place the shipping label in the upper left corner of the shipping container side.

k. Fill out the destination address label and place it in the center of the shipping container side.

2—7 PWA Packaging

The following procedure provides the necessary instructions to package a PWA for storage or shipment.

a. Obtain a quantity of antistatic bubble-wrap material (Federal Specification PPP-C-795, class 2) sufficient to wrap the PWA to a thickness of at least 1 inch. Material must be of 1/2-inch thickness, and multiple wrappings must add up to a minimum of 1 inch.

b. Wrap PWA with bubble-wrap and secure with masking tape.

c. Fill out a PWA container label per STDN No. 507, Network Logistics Manual which includes the following information:

   (1) National stock number or activity control number

   (2) Part number

   (3) Part name

   (4) Serial number

   (5) Manufacturer's name

   (6) Quantity

d. Secure the label to the wrapped PWA.

e. Place the maintenance report (when applicable) in an envelope. Identify on the envelope that it contains the maintenance report and attach the envelope to the PWA.

f. Place PWA in a cushioned shipping/storage container. The shipping/storage container should be in accordance with customer logistics procedures.

g. Place sufficient antistatic polyethylene packing material (type I) around the PWA to ensure no movement during shipment.

h. Seal the container with plastic packing tape or other suitably strong tape.

i. Fill out a shipping label per STDN No. 507, Network Logistics Manual.

j. Place the shipping label in the upper left corner of the shipping container side.

k. Fill out the destination address label and place it in the center of the shipping container side.

2–8 Storage

2–8.1 Short–Term Storage

For short-term storage the unit suffers no permanent degradation or damage when stored under the following environmental conditions:

a. Temperature: -20 to 160 degrees Fahrenheit.

b. Humidity: 0 to 100 percent relative humidity, noncondensing environment.

c. Altitude: Sea level to 35,000 feet.

2–8.2 Long–Term Storage

For long-term storage repackage the unit up to step (g) of the packaging procedure in paragraph 2-6 or 2-7. The unit suffers no permanent degradation or damage when stored under the environmental conditions specified in paragraph 2-8.1.

2–9 Shipment

Package the unit/PWA for shipment according to the procedure in paragraph 2-6 or 2-7. Ship the packaged unit by best commercial method.

Section 3 — Operation

3–1 Introduction

This section contains information and procedures to aid personnel in operating and maintaining the Integrated Receiver. A complete identification of all operating controls and indicators is included. Prior to performing maintenance, the paragraphs and procedures in this section must be understood and implemented.

WARNING

All personnel are required to read and understand paragraph 3-5, SAFETY, prior to performing any operations, removal/replacement, connections, and/or hardware tests on chassis. Failure to do so can cause death, injury, or equipment damage.

3–2 Modes Of Operation

The IR has three operating modes: online, hot standby mode, and maintenance/software delivery (offline) mode. These modes are all remotely controlled. All three equipment modes are enabled when the front panel REMOTE/LOCAL switch is in the REMOTE position (remote control), and local control is enabled when the REMOTE/LOCAL switch is in the LOCAL position (local control). The IR must be offline (front panel ONLINE indicator turned off and MAINT indicator turned on) in order to perform maintenance on the IR. The offline condition can be enabled by the TDRSS Operations Control Center No. 2 (TOCC2) operator when remote control is active or by placing the REMOTE/LOCAL switch to the LOCAL position.

3–3 Remote Control

The normal operating mode of the IR is remote control (front panel LOCAL/REMOTE switch placed in the remote position). Remote control of the IR is handled by the automated data processing equipment (ADPE) interfaced to the IR via the 1553 bus. Refer to STGT USS TOCC2 operators manual for normal/maintenance operations of the IR during remote control operation.

3–4 Local Control

Local control of the IR is strictly a maintenance mode. By placing the LOCAL/REMOTE switch in the local position, an operator is enabling the extended (offline) BIT function to be initiated from the front panel. By placing the IR in the local control condition, the unit cannot progress past the standby state (refer to section 4 for an explanation of the IR states of operation). To perform maintenance operations on the IR during local control, refer to section 5.

3–5 Safety

The following are warnings that are generally applicable when working near or inside equipment containing high voltage or other hazards that can cause death or injury and equipment damage. All warnings contained herein must be read and understood before proceeding with any removal/replacement, hardware tests, and/or connections on the IR. Throughout this manual, specific warnings, cautions, and notes appear immediately before each paragraph or procedural step to which they pertain.

WARNING

USE EXTREME CAUTION WHEN PERFORMING THE PROCEDURES IN THIS MANUAL. Contact with energized circuits can cause personal injury or death. Personnel should be familiar with CPR.

REMOVE RINGS, BRACELETS, WRISTWATCH, NECKCHAINS, AND OTHER METAL BEFORE WORKING AROUND ELECTRONIC/MECHANICAL EQUIPMENT. Jewelry can get caught and cause injury, or can cause a short circuit on contact and cause severe burns and electrical shock.

WHEN AN ABNORMAL CONDITION EXISTS AND PERTINENT PROCEDURES DO NOT APPLY, STOP THE MAINTENANCE ACTIONS AND OBTAIN EXPERT GUIDANCE. Failure to comply could lead to death or injury and equipment damage.

3–6 Equipment Access

To perform local control operations of the IR, the unit must be extended to gain access to the maintenance panel. Loosen the four captive screws holding the unit in the cabinet. Slide the unit forward until the rail guide locks are set to the locked position.

3–7 Controls And Indicators

Before proceeding with any operation with the IR, refer to paragraph 3-5. Figures 3-1 through 3-4 illustrate the various controls and indicators of the IR. Tables 3-1 through 3-5 contain a complete list of the panel operating controls and indicators, including reference designators and brief functional descriptions.

3–8 Displays And Menus

Before proceeding with any operation with the IR, refer to paragraph 3-5. The IR utilizes an interactive touch panel display which combines an alpha-numeric gas discharge dot matrix display (12x40 characters) with touch-input infrared switches. Interaction is achieved by the operator reading the display and responding by finger or pointer contact to the touch-sensitive switch location on the viewing screen. Refer to figures 3-5 through 3-24 for the IR displays.

3–9 Display Menu Hierarchy

The IR display hierarchy is as follows:

- SELECT MENU (figure 3-5)
  - MAINTENANCE MENU (figure 3-6)
    - EXTENDED BIT SUMMARY MENU (figure 3-7)
      - BIT RESULTS DISPLAY (figure 3-8)
      - OFFLINE BIT DETAIL DISPLAY (figure 3-9)
        - LRU DEFINITION DISPLAY (figure 3-10)
      - CONFIDENCE TEST RESULTS DISPLAY (figure 3-11)
        - CONFIDENCE TEST DETAIL DISPLAY (figure 3-11A)
      - ONLINE BIT RESULTS DISPLAY (figure 3-12)
      - ONLINE BIT DETAIL DISPLAY (figure 3-12A)
      - FIRMWARE VERSION DISPLAY (figure 3-13)
      - MAINTENANCE PANEL MENU (figure 3-14)
        - I CHANNEL TEST POINT SELECTION MENU #1 (figure 3-15)
        - I CHANNEL TEST POINT SELECTION MENU #2 (figure 3-16)
        - Q CHANNEL TEST POINT SELECTION MENU #1 (figure 3-17)
        - Q CHANNEL TEST POINT SELECTION MENU #2 (figure 3-18)
    - CONFIGURATION MENU (figure 3-19)
      - IR SERVICE CONFIG DISPLAY (figure 3-20)
      - IR DEMOD CONFIG DISPLAY (figure 3-21)
      - CONFIGURATION OVERRIDES DISPLAY (figure 3-19A)
    - RETURN SERVICES MENU (figure 3-22)
      - LOCK STATUS DISPLAY (figure 3-23)
      - MEASUREMENTS DISPLAY (figure 3-24)
    - ENGINEERING DISPLAY MENU (figure 3-25)
      - CARRIER ACQUISITION DISPLAY (figure 3-26)
      - CARRIER TRACKING DISPLAY (figure 3-27)
      - PN INFORMATION DISPLAY (figure 3-28)
      - SYMBOL SYNCHRONIZER DISPLAY (figure 3-29)
      - ANCILLARY PROCESSING DISPLAY (figure 3-30)

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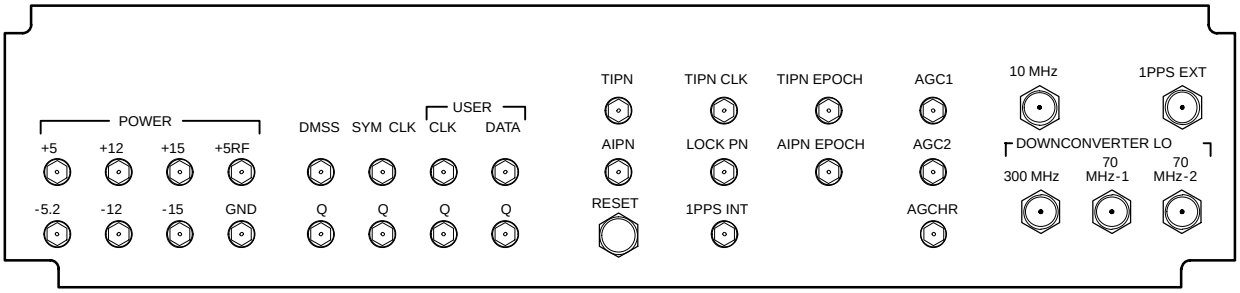

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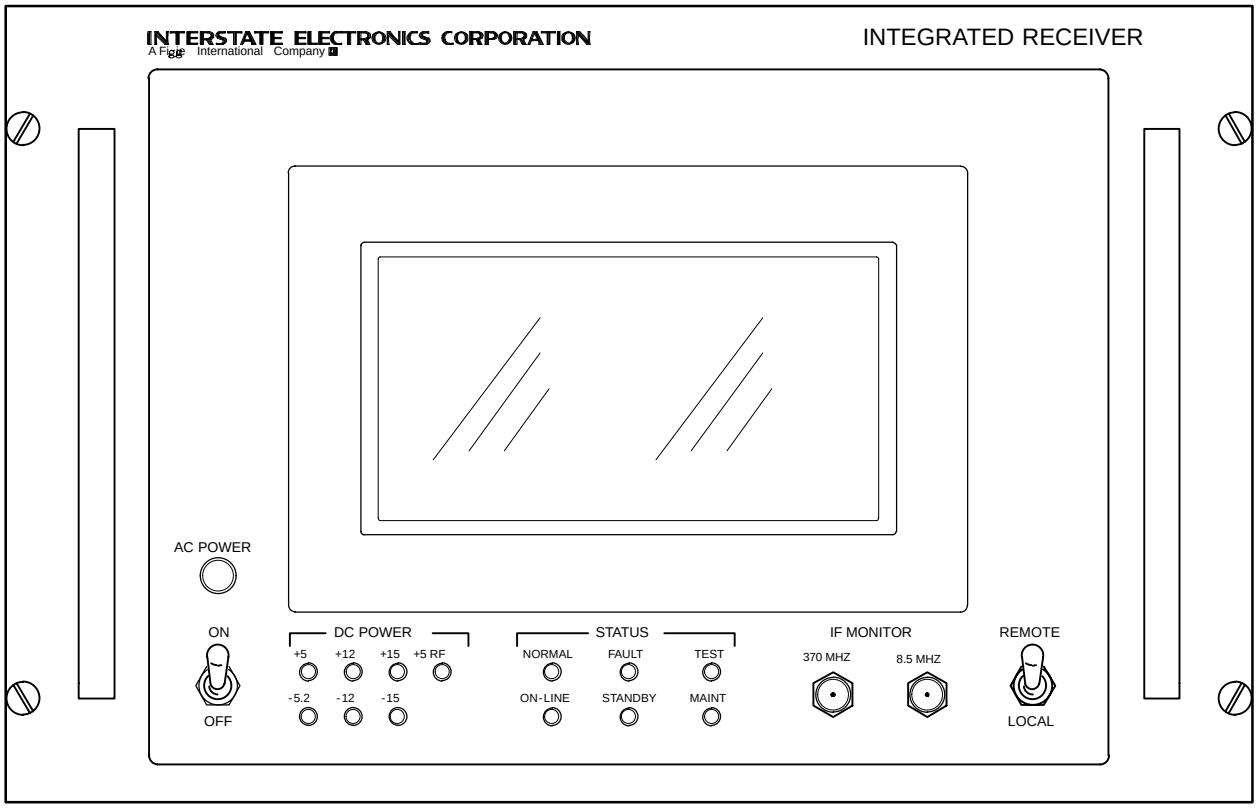


Figure 3 - 1. Front and Maintenance Panel Controls and Indicators

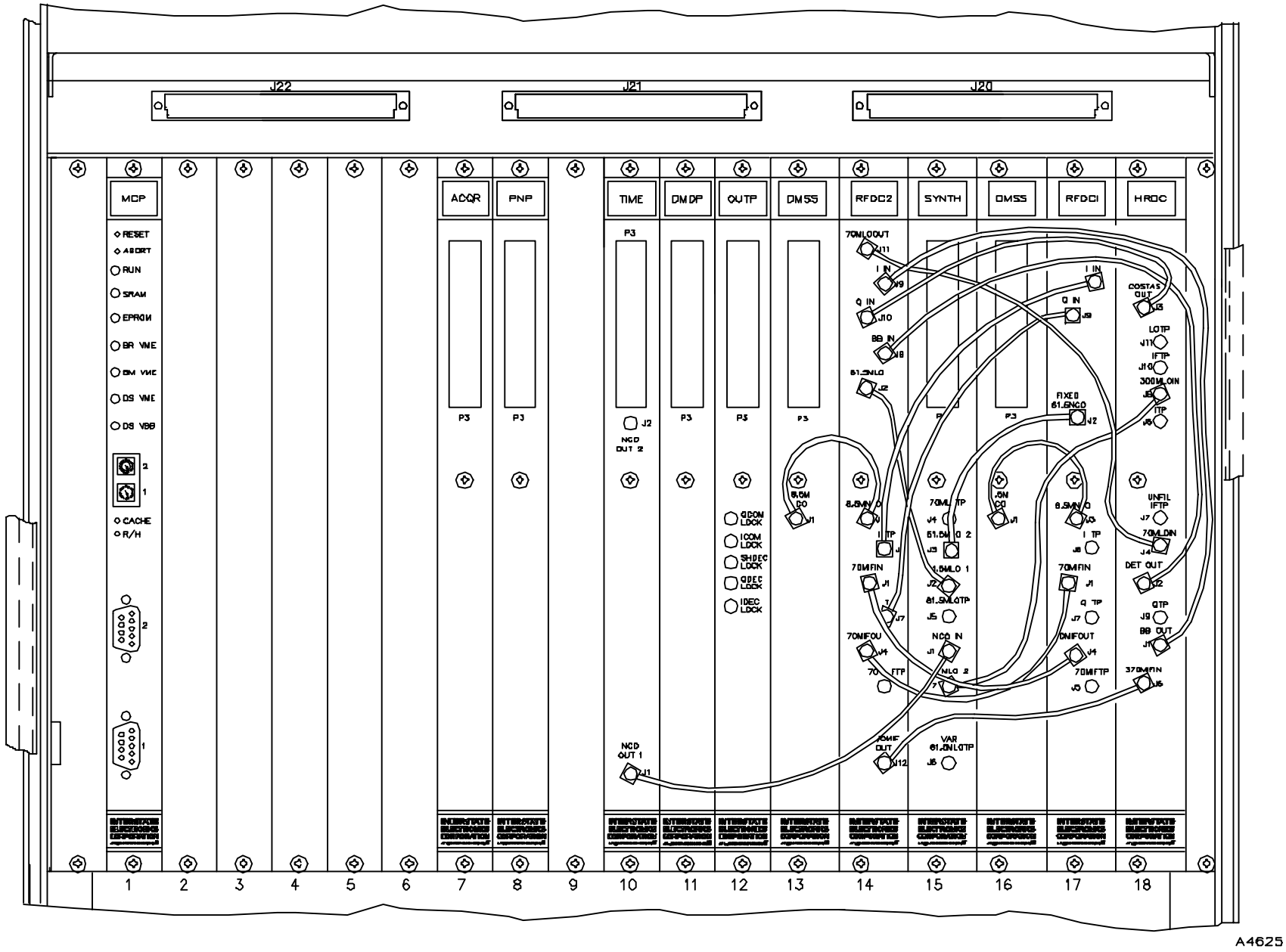
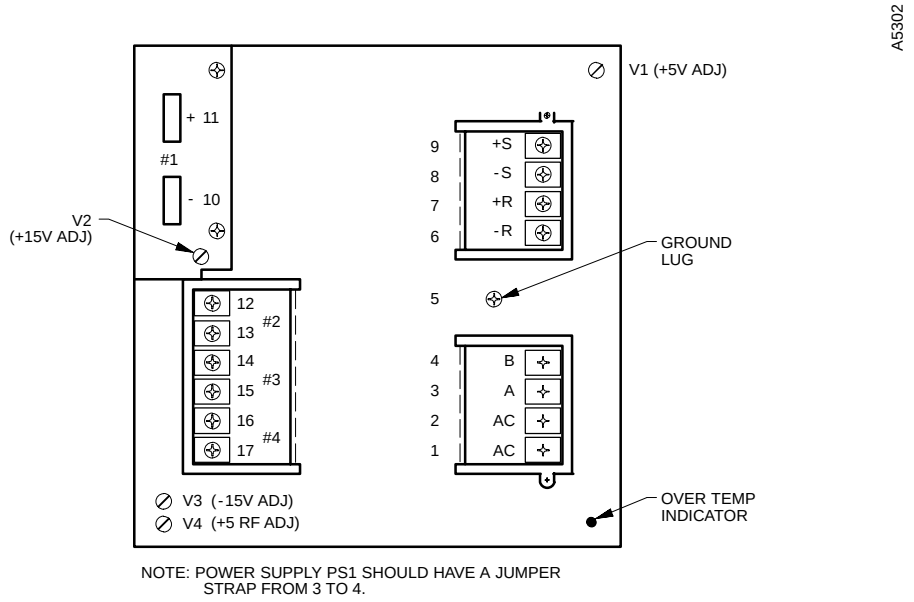
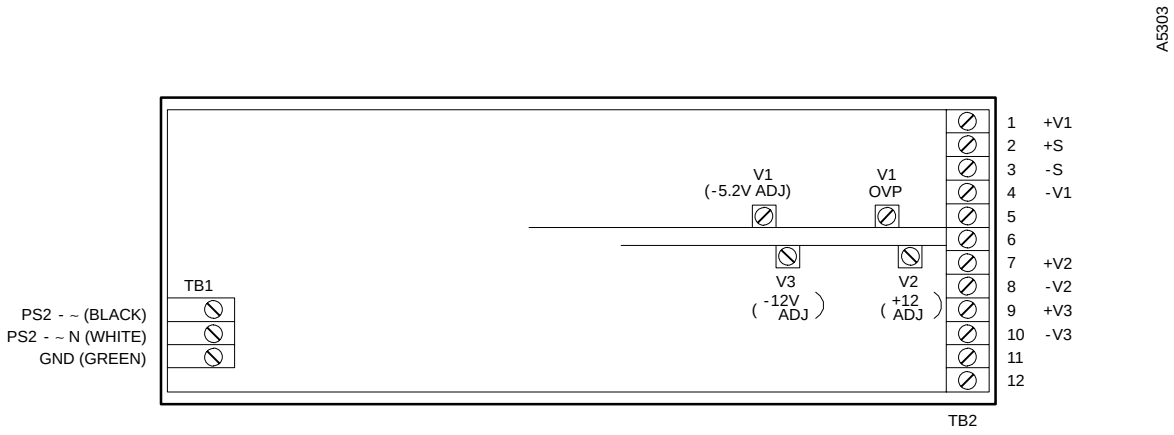


Figure 3 - 2. PWA Front Panel Controls and Indicators



NOTE: POWER SUPPLY PS1 SHOULD HAVE A JUMPER STRAP FROM 3 TO 4.

Figure 3 - 3. Power Supply No. 1 Controls and Indicators



NOTE: POWER SUPPLY PS2 SHOULD HAVE A JUMPER STRAP FROM TB2-1 TO TB2-2, AND TB2-3 TO TB2-4.

Figure 3 - 4. Power Supply No. 2 Controls

Table 3 - 1. Front Panel Controls and Indicators

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-1	“Display”	1A7A1	Touch panel display	Interactive touch panel display
3-1	AC POWER	1A7DS1	Indicator	Turns on green to indicate AC power has been distributed through unit
3-1	ON/OFF	1A7SW1	Toggle switch	Primary power on/off control
3-1	DC POWER			
	+5	1A7DS2	Indicator	Turns on green to indicate +5 Vdc power supply is activated
	+12	1A7DS3	Indicator	Turns on green to indicate +12 Vdc power supply is activated
	+15	1A7DS4	Indicator	Turns on green to indicate +15 Vdc power supply is activated
	+5 RF	1A7DS5	Indicator	Turns on green to indicate RF +5 Vdc power supply is activated
	-5.2	1A7DS9	Indicator	Turns on green to indicate -5.2 Vdc power supply is activated
	-12	1A7DS10	Indicator	Turns on green to indicate -12 Vdc power supply is activated
	-15	1A7DS11	Indicator	Turns on green to indicate -15 Vdc power supply is activated
3-1	STATUS			
	NORMAL	1A7DS6	Indicator	Turns on green to indicate that the unit is in normal operation and has passed extended BIT or confidence BIT
	FAULT	1A7DS7	Indicator	Turns on red to indicate that the unit has detected a fault as a result of the confidence, extended, or online BIT
	TEST	1A7DS8	Indicator	Turns on amber to indicate that the unit is in process of performing extended BIT or confidence BIT
	ON-LINE	1A7DS12	Indicator	Turns on green when Online Operational Light data item received from the MIL-STD-1553 interface is set

Table 3 - 1. Front Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-1	STATUS (Continued)			
	HOT-STBY	1A7DS13	Indicator	Turns on green when Standby Operational Light data item received from the MIL-STD-1553 interface is set
	MAINT	1A7DS14	Indicator	Turns on green when Maintenance Operational Light data item received from the MIL-STD-1553 interface is set
3-1	IF MONITOR			
	370 MHZ	1A7J1	Test point	Tap-off of the 370-MHz IF input to RFDC2
	8.5 MHZ	1A7J2	Test point	Tap-off of the 8.5-MHz subcarrier signal input
3-1	LOCAL/ REMOTE	1A7SW2	Toggle switch	LOCAL: Locks out the 1553 Bus interface and allows the operator to command the extended BIT from the touch panel display REMOTE: Locks out any operator control from the touch panel display and enables unit control from the 1553 Bus

Table 3 - 2. Maintenance Panel Controls and Indicators

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-1	POWER			
	+5	1A6TP1	Test point	PS No. 1 generated +5 Vdc signal
	+12	1A6TP2	Test Point	PS No. 2 generated +12 Vdc signal
	+15	1A6TP3	Test Point	PS No. 1 generated +15 Vdc signal
	-5.2	1A6TP4	Test Point	PS No. 2 generated -5.2 Vdc signal
	-12	1A6TP5	Test Point	PS No. 2 generated -12 Vdc signal
	-15	1A6TP6	Test Point	PS No. 1 generated -15 Vdc signal

Table 3 - 2. Maintenance Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-1	POWER (Continued)			
	+5 RF	1A6TP7	Test Point	PS No. 1 generated RF +5 vdc signal
	GND	1A6TP8	Test Point	Signal ground
3-1	DMSS I	1A6TP9	Test Point	Analog representation of test points 0-7 located atop the inphase DMSS PWA (card slot 16); This signal is based upon test selection
3-1	SYM CLK I	1A6TP11	Test Point	Inphase DMSS PWA demodulated symbol clock; The rising edge validates symbol data signals
3-1	DMSS Q	1A6TP10	Test Point	Analog representation of test points 0-7 located atop the quadrature DMSS PWA (card slot 13); This signal is based upon test selection
3-1	SYM CLK Q	1A6TP12	Test Point	Quadrature DMSS PWA (card slot 13) demodulated symbol clock; The rising edge validates symbol data signals
3-1	USER			
	CLK I	1A6TP15	Test Point	TTL reference clock for the selected inphase user data; The data is valid on the rising edge of this clock
	DATA I	1A6TP13	Test Point	TTL version of selected inphase user data
	CLK Q	1A6TP16	Test Point	TTL reference clock for the selected quadrature user data; The data is valid on the rising edge of this clock
	DATA Q	1A6TP14	Test Point	TTL version of selected quadrature user data
3-1	TIPN	1A6TP19	Test Point	PNP generated tracking on-time inphase PN code signal used by the DMSS Demod chip for tracking and error detection
3-1	TIPN CLK	1A6TP22	Test Point	PNP generated signal used to clock the I/Q early, on-time, and late tracking PN code signals
3-1	TIPN EPOCH	1A6TP17	Test Point	PNP generated signal used to identify start of tracking PN code (active low)

Table 3 - 2. Maintenance Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-1	AIPN	1A6TP20	Test Point	PNP generated inphase acquisition PN code signal used to drive the differential output at rear panel J108 and by the DMSS acquisition correlators
3-1	LOCK PN	1A6TP21	Test point	Bit 15 of the PNP control register; When set, signifies the MCP has code locked to the return service PN code signal
3-1	AIPN EPOCH	1A6TP18	Test point	PNP generated signal used to identify start of acquisition PN code (active low)
3-1	1PPS INT	1A6TP23	Test point	TIME generated 1-Hz TTL signal with a 20% duty cycle and valid on the falling edge; Based upon the 50-MHz signal input from the SYNTH PWA and the 1PPS external input
3-1	AGC1	1A6TP24	Test point	DMDP generated analog gain control signal used to control the RFDC1 70-MHz IF signal
3-1	AGC2	1A6TP25	Test point	DMDP generated analog gain control signal used to control the RFDC2 70-MHz IF signal
3-1	AGCHR	1A6TP26	Test point	HRDC generated analog gain control signal used to control 370-MHz IF signal
3-1	1PPS EXT	1A6J5	Connector	Connector access to 1PPS external input
3-1	10 MHZ	1A6J1	Connector	Connector access to 10-Mhz reference frequency external input
3-1	RESET	1A6SW3	Pushbutton switch	Initiates initialization and self-test of unit during any operating state
3-1	DOWN CONVERTER LO 300 MHz	1A6J4	Connector	SYNTH generated signal using the TIME generated 20-MHz signal and the internal VCXO developed 280-MHz signal; Used by RFDC2 to downconvert the return service 370-MHz signal to 70 MHz

Table 3 - 2. Maintenance Panel Controls and Indicators (Continued)

FIG REF.	PANEL MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-1	DOWN CONVERTER LO (Continued)			
	70 MHZ-1	1A6J2	Connector	RFDC1 generated signal by mixing the SYNTH generated 61.5-MHz fixed LO signal and the inphase DMSS 8.5-MHz NCO signal; Signal used in RFDC1 to quadrature downconvert the return service 70-MHz IF signal to I and Q baseband
	70 MHZ-2	1A6J3	Connector	RFDC2 generated signal by mixing the SYNTH generated 61.5-MHz fixed LO signal and the quadrature DMSS 8.5-MHz NCO signal; Signal used in RFDC2 to quadrature downconvert the return service 70-MHz IF signal to I and Q baseband

Table 3 - 3. PWA Controls and Indicators

FIG REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3-2	Modem Control Processor PWA	RESET	Switch	A reset of all onboard I/O devices and the FPCP is enabled if the RESET switch is pushed to the “up” position. RESET is held active until the switch is in the “down” position; In addition, a local timer guarantees a minimum reset time of 2 to 3 seconds; Power fail and power up also force a reset (2-3 seconds) to start the board if the supply voltage is out of range (below 4.75 volts)
		ABORT	Switch	The ABORT switch, which provides an interrupt on a software-programmable level, is provided on the board to allow an abort of the current program, to trigger a self-test, or to start a maintenance program; ABORT is activated in the “up” position and deactivated in the “down” position

Table 3 - 3. PWA Controls and Indicators (Continued)

FIG REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3-2	Modem Control Processor PWA (Cont'd)	RUN	Indicator	The RUN LED is green if the processor is not in the halt state; It is red during the reset phase or when the processor is in the halt state
		SRAM	Indicator	The SRAM LED is always lit yellow when the processor is accessing the local SRAM
		EPROM	Indicator	The EPROM LED is lit yellow when the processor accesses the EPROM area
		BR VME	Indicator	The bus request (BR) VME LED is lit yellow when the local processor requests bus mastership on the VMEbus
		BM VME	Indicator	The bus master (BM) LED is lit when the MCP is the current bus master; Optical control is provided through this LED whether or not the board is working on VME
		DS VME	Indicator	The data strobe (DS) VME LED is lit whenever the processor has placed a data strobe on the VMEbus
		DS VSB	Indicator	The DS VSB LED is lit whenever the processor has placed a data strobe on the VSB
		1, 2	Switch	The rotary switches are 4-bit hexadecimal encoded; They are completely under software control
		CACHE	Switch	The CACHE switch enables the 68030 onchip data cache with its 256 bytes when in the "down" position; In the "up" position, the onchip cache is deactivated by hardware, overriding all software settings
		R/H	Switch	The RUN/HALT (R/H) switch enables or disables local operation of the CPU and the FPCP; This switch can be used to debug multiprocessor software packages and to disable a CPU board in an application when a failure has occurred but power can't be switched off; The processor is in the halt state if the switch is in the "up" position; Normal operation is provided when the switch is in the "down" position

Table 3 - 3. PWA Controls and Indicators (Continued)

FIG REF.	PWA NAME	PANEL MARKING	TYPE OF DEVICE	FUNCTION
3-2	Synthesizer PWA	LOCK	Indicator	Turns on to indicate that the 61.5-MHz PLL, 140-MHz PLL, and 10-MHz reference input are normal
3-2	Output Processor PWA	QCOM LOCK	Indicator	Turns on to indicate that synchronization of the Q combiner is locked
		ICOM LOCK	Indicator	Turns on to indicate that synchronization of the I combiner is locked
		SHDEC LOCK	Indicator	Turns on to indicate that synchronization of the Shuttle decoder circuit is locked
		QDEC LOCK	Indicator	Turns on to indicate that synchronization of the Q decoder circuit is locked
		IDEC LOCK	Indicator	Turns on to indicate that synchronization of the I decoder circuit is locked

Table 3 - 4. Power Supply No. 1 Controls and Indicators

FIG. REF.	FIGURE MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-3	V1 (+5V ADJ)	1A2V1	Potentiometer	Used to adjust the +5.0 Vdc output voltage
3-3	V2 (+15V ADJ)	1A2V2	Potentiometer	Used to adjust the +15.0 Vdc output voltage
3-3	V3 (-15V ADJ)	1A2V3	Potentiometer	Used to adjust the -15.0 Vdc output voltage
3-3	V4 (+5RF ADJ)	1A2V4	Potentiometer	Used to adjust the +5.0 RF Vdc output voltage
3-3	OVER TEMP INDICATOR	1A2DS1	Indicator	Turns on to indicate a fan failure

Table 3 - 5. Power Supply No. 2 Controls

FIG. REF.	FIGURE MARKING	REF. DESIG.	TYPE OF DEVICE	FUNCTION
3-4	V1 OVP	1A3V1A	Potentiometer	Used to adjust the overvoltage protection threshold voltage level for the -5.2 Vdc output voltage
3-4	V1 (-5.2V ADJ)	1A3V1B	Potentiometer	Used to adjust the -5.2 Vdc output voltage
3-4	V2 (+12V ADJ)	1A3V2	Potentiometer	Used to adjust the +12.0 Vdc output voltage
3-4	V3 (-12V ADJ)	1A3V3	Potentiometer	Used to adjust the -12.0 Vdc output voltage

NOTE

THE IR DISPLAYS PROVIDE THE FOLLOWING INFORMATION:

1. eeeeeeeeeee = ERROR MESSAGES.
2. hh = { 0 to 23}; mm = { 0 to 59}; ss = { 0 to 59}.

hh:mm:ss SELECT MENU eeeeeeeeee

[ ] Maintenance

[ ] Configuration

[ ] Return Services

[ ] Engineering

[ ] Display Refresh

Figure 3 - 5. Select Menu

hh:mm:ss MAINTENANCE eeeeeeeeee

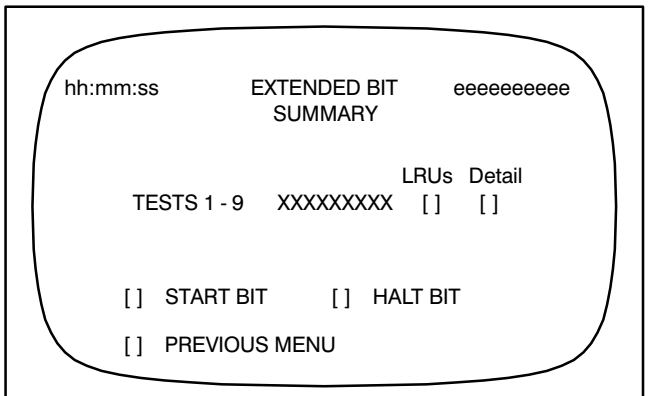
[ ] EXTENDED BIT
[ ] CONFIDENCE BIT
[ ] ONLINE BIT

[ ] DISPLAY FIRMWARE VERSION

[ ] SELECT MAINTENANCE PANEL DISPLAY

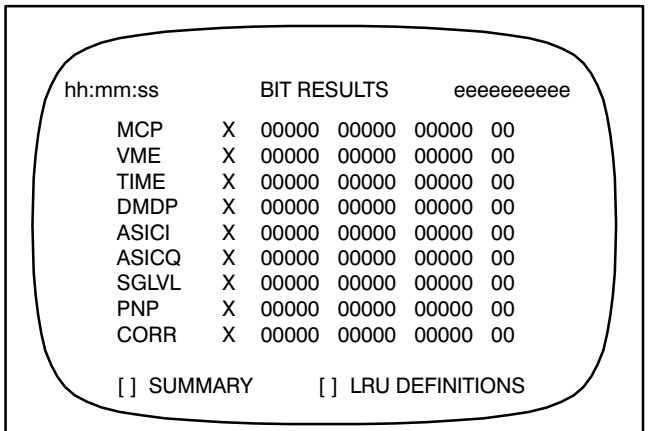
[ ] PREVIOUS MENU

Figure 3 - 6. Maintenance Menu



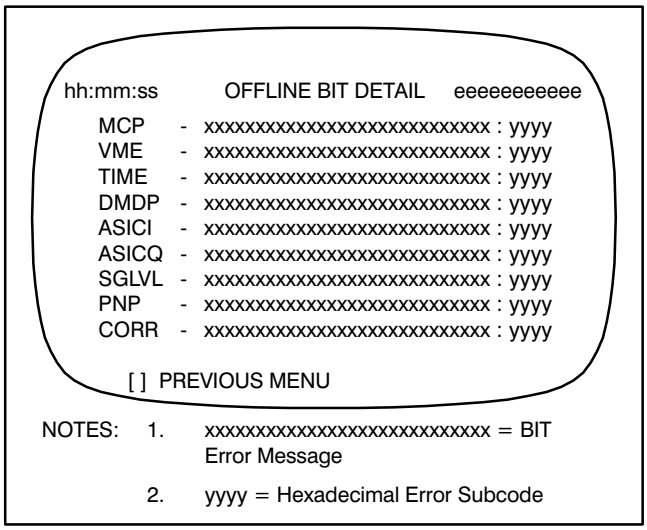
NOTES:
1. X = {" "; P; F}, WHERE " " = TEST HAS NOT RUN YET; P = TEST PASSED; AND F = TEST FAILED (ONE OR MORE BAD PWAs).
2. THE "START BIT" SELECTION IS ENABLED ONLY WHEN THE UNIT IS IN LOCAL. IF SELECTED WHEN THE UNIT IS IN REMOTE, THE ERROR MESSAGE "NOT LOCAL" IS DISPLAYED.

Figure 3 - 7. Extended BIT Summary Menu



NOTES:
1. X = {" - "; P; F}, WHERE " - " = TEST HAS NOT RUN YET; P = TEST PASSED; AND F = TEST FAILED (ONE OR MORE BAD PWAs).
2. 0 = { - ; G; S }, WHERE G = LRU GOOD; S= LRU SUSPECT; AND - = NOT APPLICABLE or TEST NOT RUN YET.
3. EACH TEST RESULT COLUMN CORRESPONDS TO AN LRU. SEE FIGURE 3-10 FOR LRU - COLUMN NUMBER CORRESPONDENCE.

Figure 3 - 8. BIT Results (Tests 1 - 8) Display



NOTES:
1. xxxxxxxxxxxxxxxxxxxxxxxxxxxx = BIT Error Message
2. yyyy = Hexadecimal Error Subcode

Figure 3 - 9. Offline BIT Detail Display

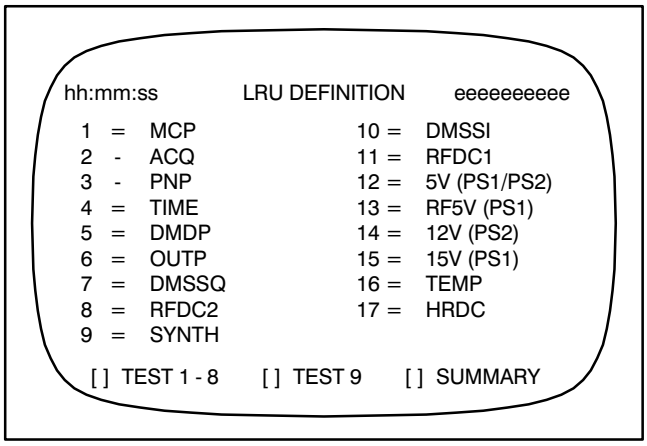
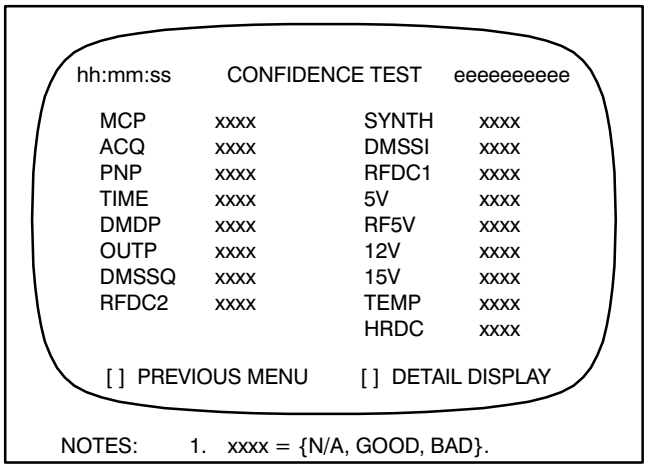


Figure 3 - 10. LRU Definition Display



NOTES:
1. xxxx = {N/A, GOOD, BAD}.

Figure 3-11. Confidence Test Results Display

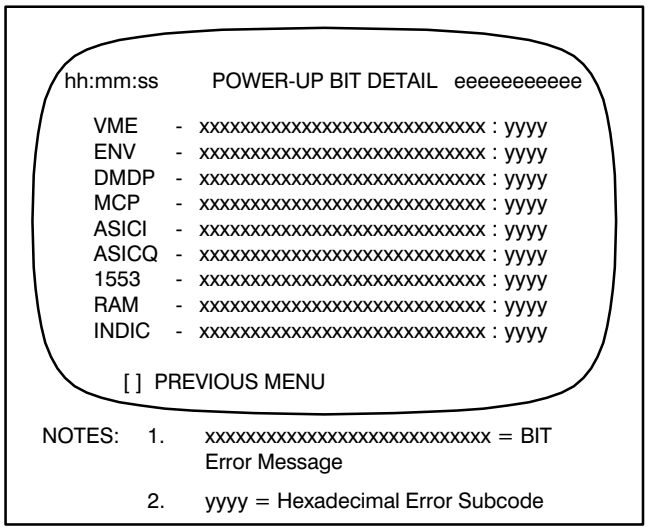


Figure 3 - 11A. Confidence Test Detail Display

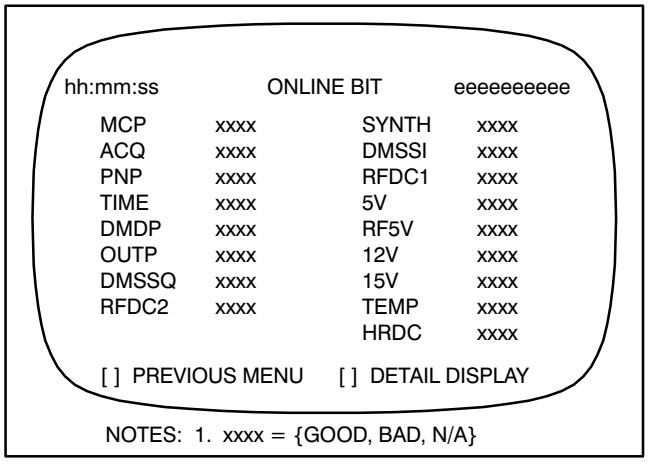


Figure 3 - 12. Online BIT Results Display

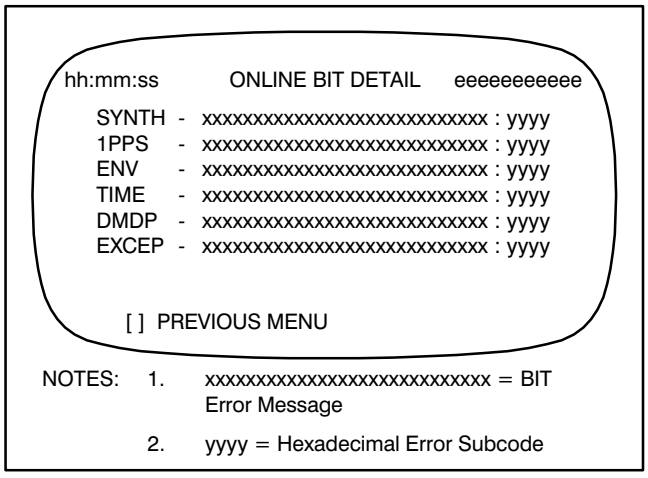


Figure 3 - 12A. Online BIT Detail Display

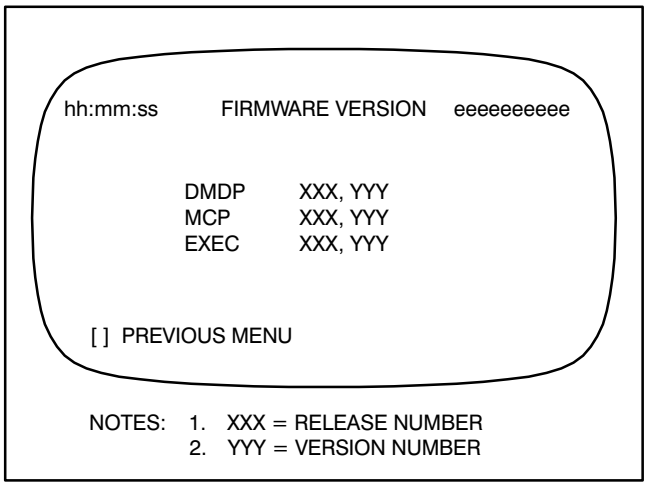


Figure 3 - 13. Firmware Version Display

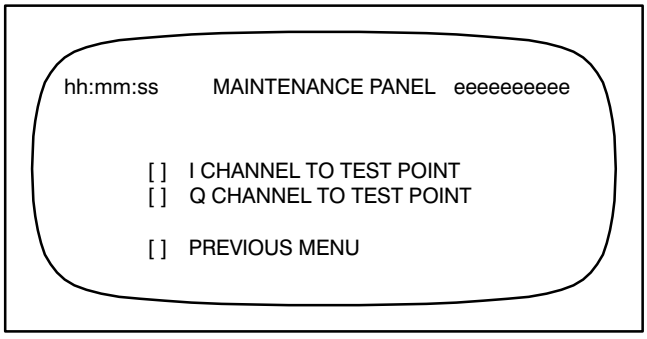


Figure 3 - 14. Maintenance Panel Menu

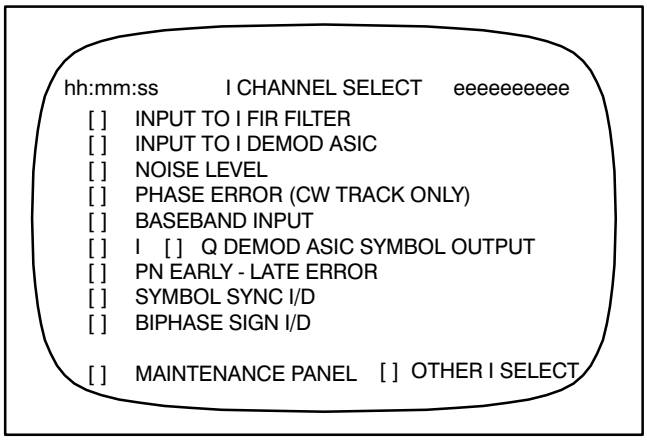


Figure 3 - 15. I Channel Test Point Selection Menu 1

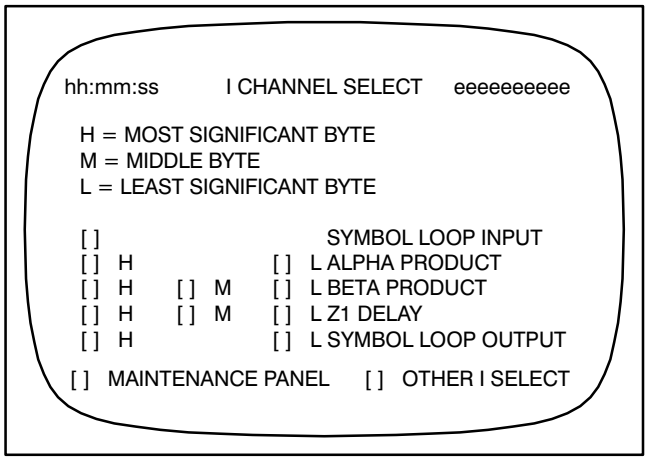


Figure 3 - 16. I Channel Test Point Selection Menu 2

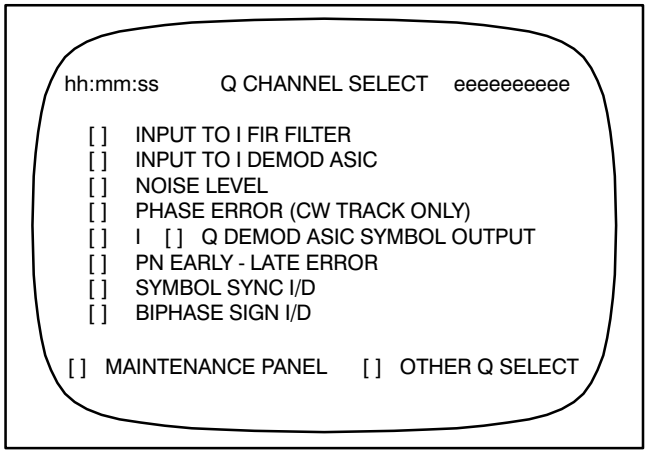


Figure 3 - 17. Q Channel Test Point Selection Menu 1

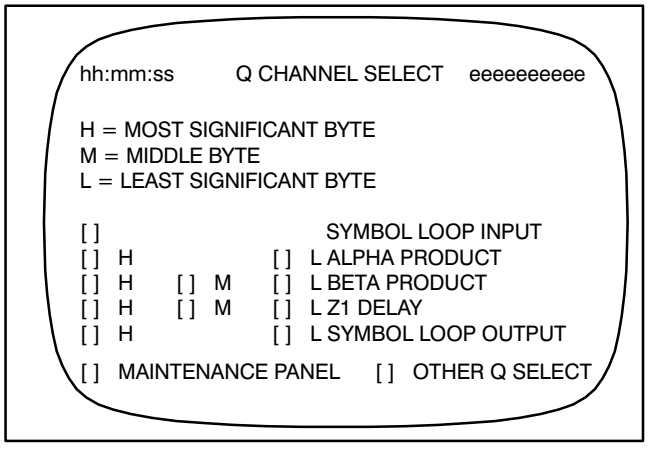


Figure 3 - 18. Q Channel Test Point Selection Menu 2

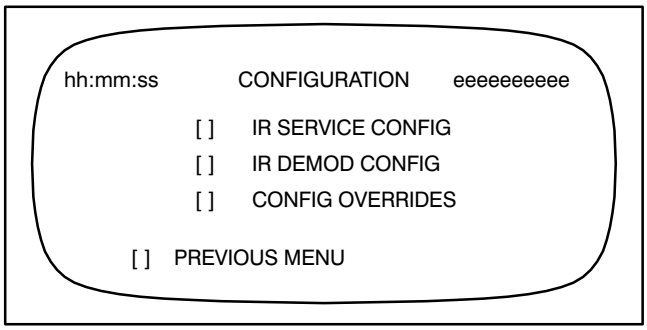


Figure 3 - 19. Configuration Menu

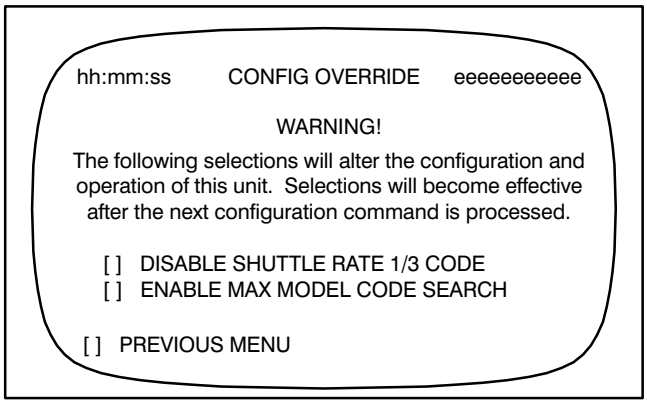
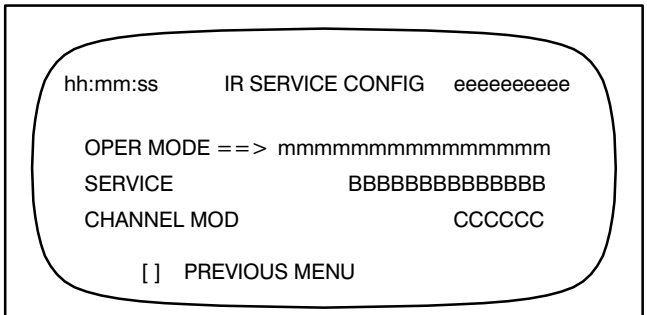


Figure 3 - 19A. Configuration Override Display



NOTES:

1. mmmmmmmmmmmmmmm = {CONFIDENCE TEST; STANDBY; EXTENDED BIT; CONFIGURED; CONFIG IN PROG; ACQUISITION; TRACK; REACQUISITION}
2. BBBBBBBBBBBBBB = {KSAR, DG1, MODE1;KSAR, DG1, MODE2; KSAR, DG1, MODE3; KSAR, DG2, MODE1; KSAR, DG2, MODE2; KSHR, MODE1; KSHR, MODE2; SSAR, DG1, MODE1; SSAR, DG1, MODE2; SSAR, DG1, MODE3; SSAR, DG2, MODE1; SSAR, DG2, MODE2; SSHR, MODE1; SSHR, MODE2; SSHR, MODE3; MAR, DG1, MODE1; MAR, DG1, MODE2; KSAF; KSHF; SSAF; SSHF, MODE1; SSHF, MODE2; MAF; MA - CAL, KSA RNG ZERO SET, SSA RNG ZERO SET, MA RNG ZERO SET}
3. CCCCCC = {SQPSK DATA, SQPSK CODE, DUAL QPSK}

Figure 3-20. IR Service Configuration Display

```
hh:mm:ss        IR DEMOD CONFIG      eeeeeeeeee

                              I              Q
DATA FORMAT                 fffff          fffff
DATA RATE               ddddddddd      ddddddd   BPS
DATA ENCODE              cccccccc       cccccccc
SYMBOL FORMAT               sss            sss
DEINTERLEAVING              iii            iii
G2 INVERSION            gggggggg       gggggggg
JITTER                      d.dd           d.dd   %
POWER IMBALANCE             X.X            X.X

  [ ]  PREVIOUS MENU
```

NOTES:
1. fffff = {NRZ - L; NRZ - M; NRZ - S; BIPHASE - L; BIPHASE - M; BIPHASE - S}
2. ddddddd = {100 to 12000000 for I; 100 to 6000000 for Q}
3. cccccccc = {UNCODED; CODE1; CODE2; CODE3; CODE4}
4. sss = {NRZ; BIPHASE}
5. x = for I: {1; 4}, for Q: {1; 2; 4}
6. iii = {ON; OFF}
7. gggggggg = {NORMAL; INVERTED}

Figure 3-21. IR Demod Configuration Display

```
hh:mm:ss        RETURN SERVICE       eeeeeeeeee

          [ ]  LOCK STATUS
          [ ]  MEASUREMENTS

       [ ]  PREVIOUS MENU
```

Figure 3 - 22. Return Services Menu

```
hh:mm:ss        LOCK STATUS          eeeeeeeeee

OPER MODE ==>                  mmmmmmmmmm
I DECODER                           11111
Q DECODER                           11111
I SYMBOL SYNC                       11111
Q SYMBOL SYNC                       11111
MAIN CARRIER                        11111
SUB CARRIER                         11111
PN CODE                             11111

  [ ]  PREVIOUS MENU
```

NOTES:
1. 111111 = {NOLOCK; LOCK}
2. mmmmmmmmmmmmmmmm = {CONFIDENCE TEST; STANDBY; EXTENDED BIT; CONFIGURED; CONFIG IN PROG; ACQUISITION; TRACK; REACQUISITION}

Figure 3 - 23. Lock Status Display

```
hh:mm:ss        MEASUREMENTS         eeeeeeeeee

MODE ==>                  mmmmmmmmmm
RANGE                  ddddddddd  ns
DOPPLER                  xddddd  Hz
I/Q CER                sd.dddd   sd.dddd
I/Q Eb/No              sd.dddd db   sd.dddd db
I/Q ACQ. TIME           ddd.dd sec    ddd.dd  sec
I/Q DATA AGC             LLLLLLLLLLL   LLLLLLLLLLL

  [ ]  PREVIOUS MENU
```

NOTES:
1. d.dddd = Float; s = {+ or - }; dd = Exp value.
2. mmmmmmmmmmmmmmmm = {CONFIDENCE TEST; STANDBY; EXTENDED BIT; CONFIGURED; CONFIG IN PROG; ACQUISITION; TRACK; REACQUISITION}
3. LLLLLLLLLL = {LEVEL LOW, LEVEL OK, LEVEL HIGH}

Figure 3 - 24. Measurements Display

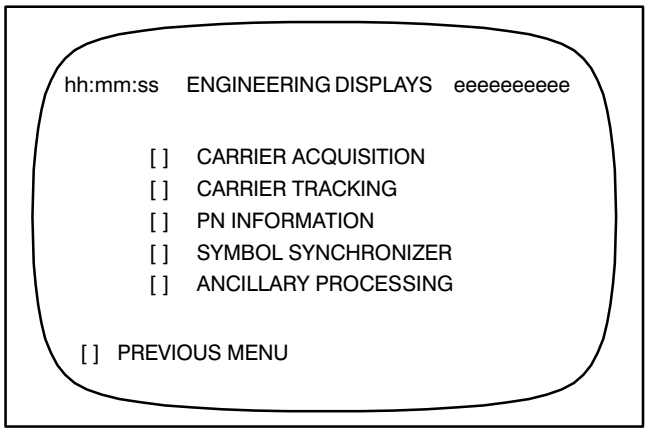
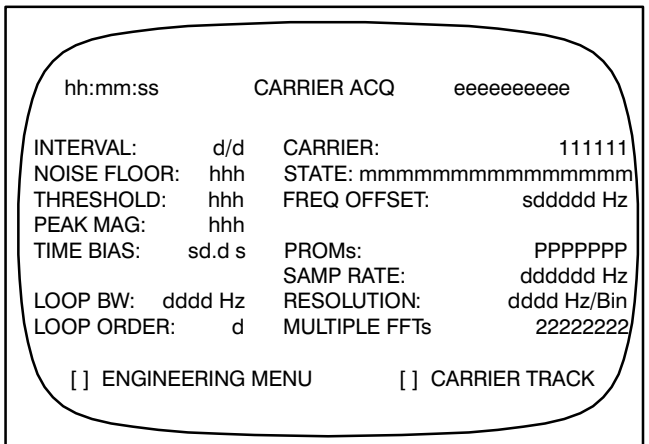
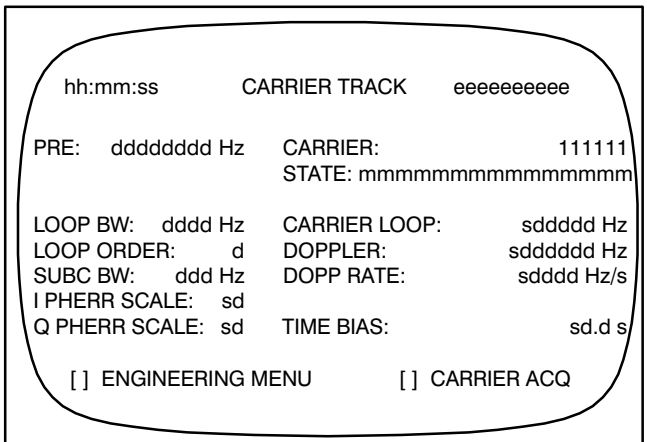


Figure 3 - 25. Engineering Display Menu



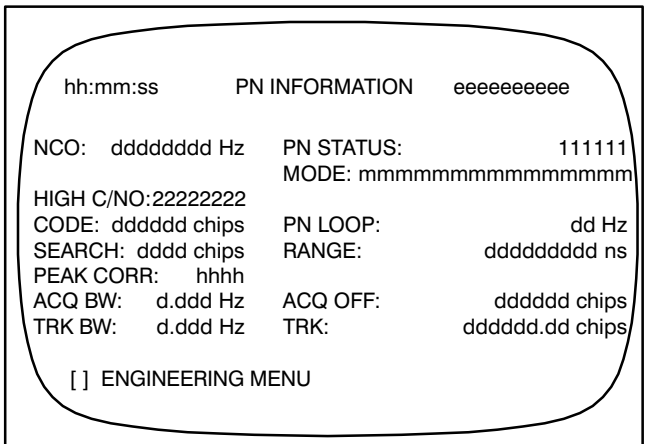
NOTES:
1. d = Integer; d.d = Float; s = {+ or - }; h = Hex
2. 111111 = {NOLOCK; LOCK}
3. mmmmmmmmmmmmmmmm = {CONFIDENCE TEST; STANDBY; EXTENDED BIT; CONFIGURED; CONFIG IN PROG; ACQUISITION; TRACKING; REACQUISITION}
4. PPPPPPP = {SQUARE; QUAD; NONE}
5. 22222222 = {ENABLED; DISABLED}

Figure 3 - 26. Carrier Acquisition Display



NOTES:
1. d = Integer; d.d = Float; s = {+ or - }
2. 111111 = {NOLOCK; LOCK}
3. mmmmmmmmmmmmmmmm = {CONFIDENCE TEST; STANDBY; EXTENDED BIT; CONFIGURED; CONFIG IN PROG; ACQUISITION; TRACKING; REACQUISITION}

Figure 3 - 27. Carrier Tracking Display



NOTES:
1. d = Integer; d.d = Float; h = Hex
2. 111111 = {NOLOCK; LOCK}
3. mmmmmmmmmmmmmmmm = {CONFIDENCE TEST; STANDBY; EXTENDED BIT; CONFIGURED; CONFIG IN PROG; ACQUISITION; TRACKING; REACQUISITION}
4. 22222222 = {ENABLED; DISABLED}

Figure 3 - 28. PN Information Display

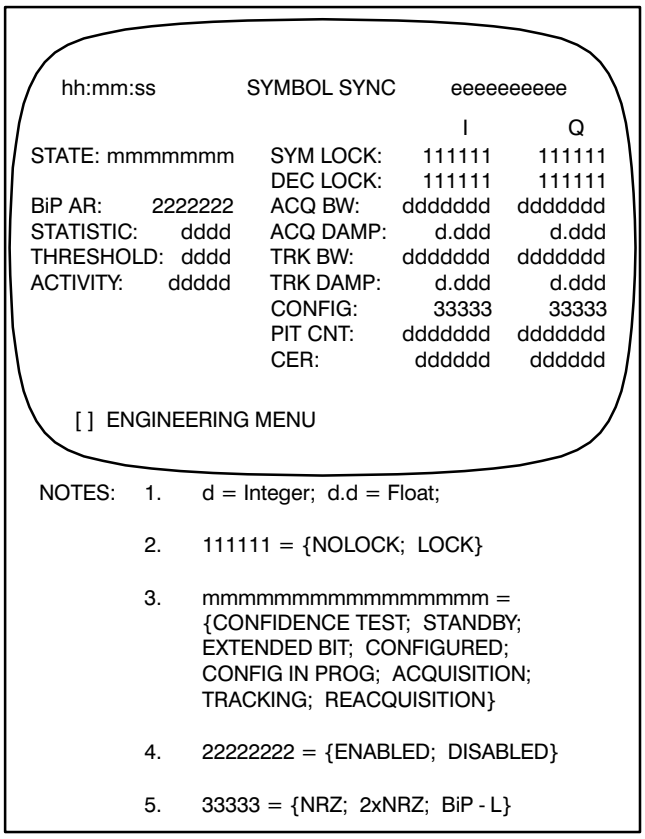


Figure 3 - 29. Symbol Synchronizer Display

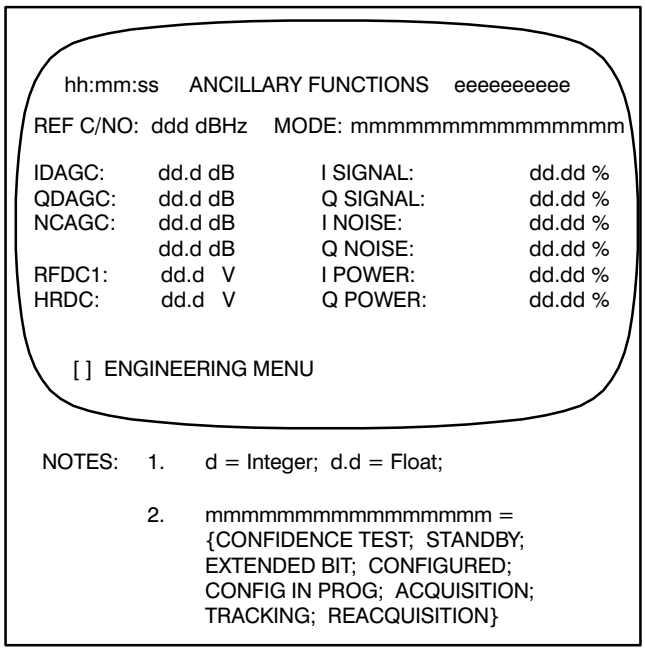


Figure 3 - 30. Ancillary Processing Display

Below is a list of explanations for display/operator interaction.

a. An invalid touch key selection produces an "INVALID SELECTION" message in the right upper hand top corner of display.

b. The bottom left corner of each returns the display to the previous menu level. If the menu level is zero (highest), then touching the bottom left corner results in the display being refreshed.

c. The upper left corner of every display contains the current time of day.

d. The selected display is updated once every second.

3–10 Display Error Messages

Table 3-6 contains the possible IR display error messages and descriptions that may occur during operation of the unit.

3–11 Self–Check

Before proceeding with any operation of the IR, refer to paragraph 3-5. The following procedures pertain to operating the IR under local control. Refer to STGT USS TOCC2 operators manual for normal and maintenance operating procedures performed from the TOCC2 console by the TOCC2 operator (remote control). Refer to the applicable O&M manual for maintenance procedures within suspect ambiguity group, but not accomplished by the TOCC2 operator (performed by the line maintenance technician (LMT) utilizing the maintenance test group (MTG)). The applicable STGT manual numbers and titles are:

a. MA Forward O&M Manual; 530-STGT-O4006.

b. MA Return O&M Manual; 530-STGT-O4005.

c. SSA Forward O&M Manual; 530-STGT-O4002.

d. KSA Forward O&M Manual; 530-STGT-O4004.

3–12 Turn–On

The IR requires no special actions to be taken when turning on a newly installed IR assembly. Turn on the IR by placing the ON/OFF switch to the ON position. Verify the AC POWER and DC POWER indicators turn on and the SELECT MENU appears.

Table 3 - 6. Display Error Messages	
ERROR MESSAGES	DESCRIPTION
INVALID SEL	Notifies the operator that an illegal area on the front panel display was touched; Processing continues awaiting legal operator interaction
NOT LOCAL	Notifies the operator that front panel initiation of the extended BIT function occurred while the Integrated Receiver was in the remote mode; Processing continues awaiting legal operator interaction
BIT RUNNING	Notifies the operator that the BIT function is presently executing and Integrated Receiver operations are halted until completion of the BIT function

3–13 Built–In Test

3–13.1 The IR employs three levels of self-check built-in test (BIT) features. The first-level BIT (confidence BIT) is performed at powerup and reset of the unit (see paragraph 3-18). The second-level BIT (online BIT) is performed continuously during all operational states of the IR (see paragraph 3-19). The third-level BIT (extended BIT) is performed upon command (from ADPE during remote control or front-panel display (EXTENDED BIT SUMMARY MENU; figure 3-7) during local control) (see paragraph 3-20).

3–13.2 While in remote control, extended BIT can be commanded during any IR operational state. Refer to section 5, paragraph 5-6 for procedures concerning initiation of IR BIT functions while in the local control condition. Refer to STGT USS TOCC2 operators manual for initiation of the IR BIT functions while in the remote control condition.

3–14 Normal Operation

Refer to STGT USS TOCC2 operators manual and the TOCC2 operator for operating the IR during normal (remote control) conditions.

3–15 Emergency Operation

Refer to STGT USS TOCC2 operators manual and TOCC2 operator for operating IR during emergency conditions.

3–16 Shutdown

Secure the IR by placing the ON/OFF switch in the OFF position. Verify the AC POWER and DC POWER indicators turn off.

3–17 BIT Features

The IR employs three levels of BIT features. Refer to the following paragraphs for explanations of the specific functions performed:

a. Confidence BIT: 3-18.
b. Online BIT: 3-19.
c. Extended BIT: 3-20.

3–18 Confidence Bit

The IR runs initialization and self-test routines (confidence BIT) at powerup or unit reset. Upon initiation of the confidence BIT, the front panel TEST indicator is turned on. If any routine does not complete successfully, the FAILURE indicator is turned on and the IR halts operation and/or sets the applicable LRU fail status. Upon successful completion of the confidence BIT, the TEST indicator is turned off, and the IR enters the standby state. The routines are as follows:

a. System random access memory (RAM) test.
b. Central processing unit (CPU) test.
c. Kernel initialization.
d. Interrupt initialization
e. MIL-STD-1553 test.
f. I/O initialization.
g. VME test.
h. DMDP test.
i. Demod application specific integrated circuit (ASIC) test.
j. Environment test.
k. Indicators test.

3–18.1 RAM Test

This test performs four different write, read, and compare operations on the MCP RAM. The RAM test uses a 5's pattern, an A's pattern, an address pattern, and inverse address pattern to determine the RAM health. If any RAM locations fail the front panel FAULT LED is turned on, the status register is loaded with a RAM fail indication, and processing is halted.

3–18.2 CPU Test

This test performs four different tests on the MC68030 CPU resident on the MCP PWA. The first test verifies operation of the CPU data, address, and control registers. The second test verifies operation of the CPU's instruction set. The third test verifies operation of the CPU addressing modes. The fourth test verifies operation of CPU exception processing, including the following exceptions: bus error, address error, illegal instruction, zero division, check instruction, TRAPV instruction, privilege violation, trace, trace on change, line-A emulation, line-F emulation, format error, and the 16 software traps. If any CPU test fails, the front panel FAULT LED is turned on, the status register is loaded with a CPU fail indication, and processing is halted.

3–18.3 Kernel Initialization

This function creates the kernel system environment using the values supplied in the kernel configuration table. Once the kernel pointers have been set up, the kernel workspace is set up, the task control blocks are created, the user stacks are set up, the interrupt service routine (ISR) stacks are created, and the internal kernel variables are initialized. If any of the kernel initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start-fail indication, and processing is halted.

3–18.4 Interrupt Initialization

This function initializes the interrupt circuitry to allow hardware interrupts to the MCP. All device generated interrupt vectors and autovectors are initialized in the exception vector table during this routine. If any of the interrupt initialization tasks fail, the front panel FAULT LED is turned on, the status register is loaded with a start-fail indication, and processing is halted.

3–18.5 MIL–STD–1553 Test

This function verifies operation of a DDC bus-61553 MIL-STD-1553 device. Tested features include buffer RAM, device configurability, and data transmission/reception in an internal loopback mode. The buffer RAM test writes, reads, and compares 5's, A's, address, and inverse address test patterns. The device configurability test writes, reads, and compares a configuration test pattern to the registers and then resets the registers and reads their reset value. The loopback test sets up the TIME for 1553 operation, loads test data messages, and instructs the 1553 device to transmit the data. If the data does not transmit correctly or during a specified time, the front panel FAULT LED is turned on.

3–18.6 I/O Initialization

This function initializes the MIL-STD-1553 remote terminals and RS-232C device to a known state and verifies that state. If any of the I/O initialization tasks fail, the front panel FAULT LED is turned on.

3–18.7 VME Test

This function verifies proper operation of the PNP, TIME, ACQR, and DMDP VME data transfer bus. A test data word is written to and/or read from each of the testable PWAs. If a bus exception occurs during access, the test fails. On the PWAs that have read/write capabilities, a test word is written to the PWA, read back from it, then compared to the expected word. If the words do not compare, the VME bus test fails. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.8 DMDP Test

3–18.8.1 This function performs two independent tests on the DMDP. The first test is an internal self-test feature and the second is testing the DMDP resident RAM. The selftest is controlled by the DMDP TMS processor and verifies operation of itself, FFT device, and operation of the DMDP RAM. The TMS functions tested are: internal register operation, addressing modes, instruction set operation, interrupt processing, and interrupt of the MCP.

3–18.8.2 The second test is called the TMS/MCP dual ported RAM (DPRAM) test. The DPRAM is tested by four write/read data patterns: 5's, A's, address, and inverse address. The 5's and address patterns are written by the MCP and read/validated by the TMS. The A's and inverse address patterns are written by the TMS and read/validated by the MCP. This test fails if any test data read from the DPRAM does not correspond to the test data written to the DPRAM. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.9 Demod ASIC Test

This function performs an ASIC signature test. The MCP commands the DMDP to perform an ASIC signature test and then waits for a timeout. If the DMDP responds incorrectly, the DMDP is flagged as faulty and the test is stopped but processing continues. Next the MCP evaluates the result of the signature test. Incorrect test results flag the DMSS at faulty. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.10 Environment Test

This function verifies proper operation of the TIME PWA's analog-to-digital (A/D) converter and proper voltage and temperature levels. The TIME status register is read for proper bit settings. If the WRAM bit is not set the test fails. With the WRAM bit set, the test reads the TIME digitized voltage values for 5 Vdc, RF 5 Vdc, 12 Vdc, 15 Vdc, and the unit temperature. If any of these environmental parameters are not within their specified normal ranges, the test fails. Processing continues regardless of outcome. The FAULT indicator is turned on if the test failed and status can be determined via the CONFIDENCE TEST RESULTS DISPLAY (figure 3-11).

3–18.11 Indicators Test

This function verifies proper indicator operation by turning all VMEbus-controlled indicators on for one second. Verification of proper operation is by visual inspection of the indicators while they are turned on.

3–19 Online Bit

Online BIT is a function of the schedule 1-second tasks. Online BIT is run as a continuous process, once per second, during all active IR states. The routines are as follows:

a. Monitor CPU exceptions.
b. Monitor time.
c. Monitor environment.
d. Monitor synthesizer lock.
e. Monitor TMS Status
f. Monitor 1 PPS.

3–19.1 Monitor CPU Exceptions

This function continually monitors any unexpected CPU exceptions which would set an MCP LRU failure, RS-232 channel 1 or 2 error status/spurious interrupt that would set an MCP LRU failure, and the 1553 bus channel 1 error status/spurious interrupt that would set a TIME LRU failure. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.2 Monitor Time

This function monitors the 1-second, 100-millisecond, 10-millisecond, and 1-millisecond interrupts and compares them to relative nominal values. If this value varies by more than one count, the TIME LRU is flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.3 Monitor Environment

This function verifies proper operation of the TIME PWA's A/D converter (ADC) and proper voltage and temperature levels. The TIME status register is read for proper bit settings. If the WRAM bit is not set the test fails. With the WRAM bit set, the test reads the TIME digitized voltage values for 5 Vdc, RF 5 Vdc, 12 Vdc, 15 Vdc, and the unit temperature. If any of these environmental parameters are not within their specified normal ranges, the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.4 Monitor Synthesizer Lock

This function checks the Reference 10-MHz bit for assertion and either of the 140-MHz or 61.5-MHz bits for non-assertion. Any of these conditions cause the SYNTH LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.5 Monitor TMS Status

This function checks the status of the TMS/MCP interface by sampling the DMDP Time Tag Error bit for a true setting or that the DMDP Command Rejection Count register value is not zero. Next, the unit state and TMS operational mode are used to set up a two dimensional state validation matrix and then compared. Four consecutive inconsistent comparisons set a fault flag. Any of these fault conditions cause the DMDP LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–19.6 Monitor 1 PPS

This function samples the Synchronization Complete bit and the Synchronization Error bit for a true setting. This condition causes the TIME LRU to be flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status can be determined via the ONLINE BIT RESULTS DISPLAY (figure 3-12).

3–20 Extended Bit

The extended BIT is executed only upon command via the 1553 interface (remote control) or front panel (local control). While extended BIT is in progress, all other IR functions, except those which maintain time, are paused. Upon completion of extended BIT, the unit returns to the standby state. The extended BIT routines are broken up into two groups; group 1 routines are the basic functions tests and group 2 routines are the receiver functions tests. The basic functions test routines are as follows:

a. MCP Test (Test 1).

b. VME Test (Test 2).

c. DMDP Test (Test 3).

d. TIME Test (Test 4).

e. Signal Levels Test (Test 5).

f. Demod ASIC Test (Test 6).

The receiver functions test routines are as follows:

g. PNP Test (Test 7).

h. Correlator Tap Test (Test 8).

i. DC Bias Test (Test 9).

3–20.1 MCP Test

3–20.1.1 The MCP test passes if both subtests pass; the 68030 subtest and programmable interval timer (PIT) subtest. The 68030 subtest performs four different tests on the MC68030 CPU. The first test verifies operation of the CPU data, address, and control registers. The second test verifies operation of the CPU's instruction set. The third test verifies operation of the CPU addressing modes. The fourth test verifies operation of CPU exception processing.

3–20.1.2 The second subtest verifies operation of the two MCP PITs. This subtest tests the PIT's registers, timers, and interrupts. The registers are tested by writing and reading a test word to/from each register and verifying that the word read from the register is the same as the word written to the register. The two PIT timers are tested by comparing their measurement of a short period of time. This subtest fails if a register data write/read is inconsistent, or if the PIT timers do not measure a period of time within +/- 5% of each other, or if the PIT interrupts do not occur. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 1) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.2 VME Test

The VME test verifies operation of the VME data transfer bus. A test data word is written to and/or read from each of the VME slave LRUs (PNP, ACQR, TIME, and DMDP). If a bus exception occurs during LRU access, this test fails. On those LRUs that have a write/read capability, a test word is written to the LRU and then compared to the test word read from that LRU. If the test data words do not compare, this VME bus test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 2) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.3 DMDP Test

3–20.3.1 The DMDP test performs two independent tests on the DMDP. The first test is an internal self-test feature and the second tests the DMDP resident RAM. The selftest is controlled by the DMDP TMS processor and verifies operation of itself, FFT device, and operation of the resident RAM. The TMS functions tested are: internal register operation, addressing modes, instruction set operation, interrupt processing, and interrupt of the MCP.

3–20.3.2 The second test is called the TMS/MCP DPRAM test. The DPRAM is tested by four write/read data patterns: 5's, A's, address, and inverse address. The 5's and address patterns are written by the MCP and read/validated by the TMS. The A's and inverse address patterns are written by the TMS and read/validated by the MCP. This test fails if any test data read from the DPRAM does not correspond to the test data written to the DPRAM. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 3) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.4 Time Test

The TIME test performs two independent tests on the TIME PWA. The first test verifies that the four timing interrupts (1-, 20-, 100-, and 1000-pps time marks) occur within a specified tolerance. The second test verifies that the 5.0 Vdc reference signal is within a specified tolerance. The intervals of the timing interrupts are measured by a PIT counter and the 5 Vdc reference input to the TIME ADC is converted to a digital representation and verified. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 4) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.5 Signal Levels Test

The signal levels test verifies that a DC bias can be compensated for, and that the rms I and Q signal levels are within +/- 5% of each other, when measuring a test signal. This test verifies the signal levels through five data paths in the IR. The MCP selects a 70-MHz test signal and commands the TMS processor to perform a DC bias procedure. The MCP then verifies that the new bias values have not varied more than a specified tolerance amount from their previous values. The MCP then configures the TMS processor for a carrier NCO offset of 1000 Hz from its 8.5-MHz frequency, with a sample rate of 5-Hz bin width. The MCP commands the TMS processor to acquire and after acquisition is achieved, reads the rms magnitude of the I and Q signals from the TMS processor. The I and Q signal magnitudes are compared by the MCP to determine test results as defined above. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 5) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.6 Demod ASIC Test

This test performs an ASIC signature test. The MCP commands the DMDP to perform an ASIC signature test and then waits for a timeout. If the DMDP responds incorrectly, the DMDP is flagged as faulty and the test is stopped but processing continues. Next the MCP evaluates the result of the signature test. Incorrect test results flags the DMSS as faulty. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 6) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.7 PNP Test

This test configures the PNP to generate PN codes, and to cause an interrupt at epoch occurrence. The PN codes at the epoch are sampled to verify their values. Acquisition and track epoch interrupts are timed to verify that they occur within a specified tolerance time interval. If any sampled PN codes are not as expected, or if an epoch interrupt does not occur or occurs outside of the tolerance, the test fails. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 7) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.8 Correlator Tap Test

This test configures the PNP with values of coherent and non-coherent signal combination parameters and NCO parameters. The correlator tap test passes if each of four selected taps yield expected peak indices and bin magnitudes, and if a peak detect interrupt occurs within a specified period of time. Unexpected peak indices, bin magnitudes or peak detect interrupts cause the test to fail. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 8) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

3–20.9 DC Bias Test

This test compares dc offset values as determined by the TMS with values measured by the TIME ADC. If the values do not compare within a specified tolerance, or if the measured values change, the test fails and the DMDP is flagged as suspect. The FAULT indicator is turned on if a failure occurs. Processing continues regardless of outcome and status (Test 9) can be determined via the EXTENDED BIT SUMMARY, BIT RESULTS, and LRU DEFINITIONS displays (figures 3-7 through 3-10).

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Section 4 — Theory Of Operation

4-1 Introduction

This section provides a functional description of the Integrated Receiver (IR). A general functional description is presented at the block diagram level, followed by individual detailed descriptions of the unit's major functions and hardware/firmware components. The detailed descriptions are supported by timing, flow, logic, and schematic diagrams, when necessary. The information contained in this section is keyed to the Level 1 maintenance procedures in section 5.

4-2 Detailed Functional Description

The IR processes all SSA, MA, KSA low data rate return data and KSA high data rate return data for the STGT USS. Having the capability of supporting each of these configurations, the IR can be used interchangeably in any of the unique configuration equipment groups. Although the IR supports the above mentioned configurations, not all of the IR functional capabilities are required for each. Refer to figure 4-1 for the following functional descriptions.

4-3 Firmware Descriptions

The IR contains three distinct firmware programs: the executive program (Exec), the MCP program, and the DMDP program. The MCP and DMDP programs are application programs that provide the necessary scheduling and control of the IR during operation. The executive program provides I/O services for the MCP application program.

4-3.1 Executive Program

The Exec provides the application programs with a real-time operating system. The operating system provides multi-tasking and resource management of unit input/output. Part of the Exec consists of the VRTX32 multi-tasking kernel that provides the multi-tasking scheduling and memory resource management functions. The Exec is comprised of the following function design units (FDUs) and together combine to provide an integrated interface between the hardware and the application programs:

a. Power-On and Exec Initialization. This FDU is started by either a hardware reset or an application call execute command (Excmd) to reinitialize. When this occurs, this FDU checks the system RAM, boots all code into the system RAM and then starts operation from system RAM. The system kernel is initialized, the event vector table is setup, and I/O devices are initialized. Finally, the I/O devices are tested as part of the online BIT FDU and the application program is started.

b. Input/output. I/O FDUs (RS-232 and MIL-STD-1553) typically have two entry points that consist of functions that the applications call (i.e., Exec Read and Exec Write) and interrupt service routines (ISRs) that are invoked by the hardware generated interrupts. The application programs use the I/O FDUs to interface to the system I/O hardware.

c. Event Handlers. This FDU provides the interrupt service routines for the signal processing and timing hardware interrupts that schedule the time critical signal processing.

d. Exception Handlers. This FDU interfaces the MC68030 to error processing and recovery ISRs. These ISRs also allow for report generation that details the error that was encountered.

e. Download Code. This FDU provides the capability of downloading software code to the MCP processor. Ephemeris data download is also included in this FDU. The download is via the MIL-STD-1553 bus.

f. Exec BIT. This FDU provides confidence tests for the I/O devices that can be called by the power-on and Exec initialization FDU or by the application program.

4-3.2 MCP Program

The MCP program is the master application program of the IR. The MCP program's purpose is to configure and control acquisition and tracking of the carrier and PN code of the return service signal. It also provides status updates to the ADPE via the MIL-STD-1553 bus interface. The IR is remotely controlled via the 1553 bus interface and as master program, provides any data required by the DMDP processor. The MCP program also interfaces with TIME, front panel (via an RS-232 interface), PNP, and ACQR. The MCP program is comprised of the following functions:

a. Command Processor Function. The command processor function processes the commands received over the 1553 bus from the ADPE. Commands over the 1553 bus are received asynchronously, and this function processes each command upon receipt. Some commands contain an effective time which determines when the action defined within the command is to take place. On startup, this function clears the 1553 bus interface and initiates input from the 1553 bus and processes that input. Verification is made that the LOCAL/REMOTE switch is in the REMOTE position before processing any commands. When applicable, the ephemeris database is updated. This function is capable of filling the ephemeris database to its maximum size of 50 minutes with a limit of ten minutes of ephemeris data per transfer.

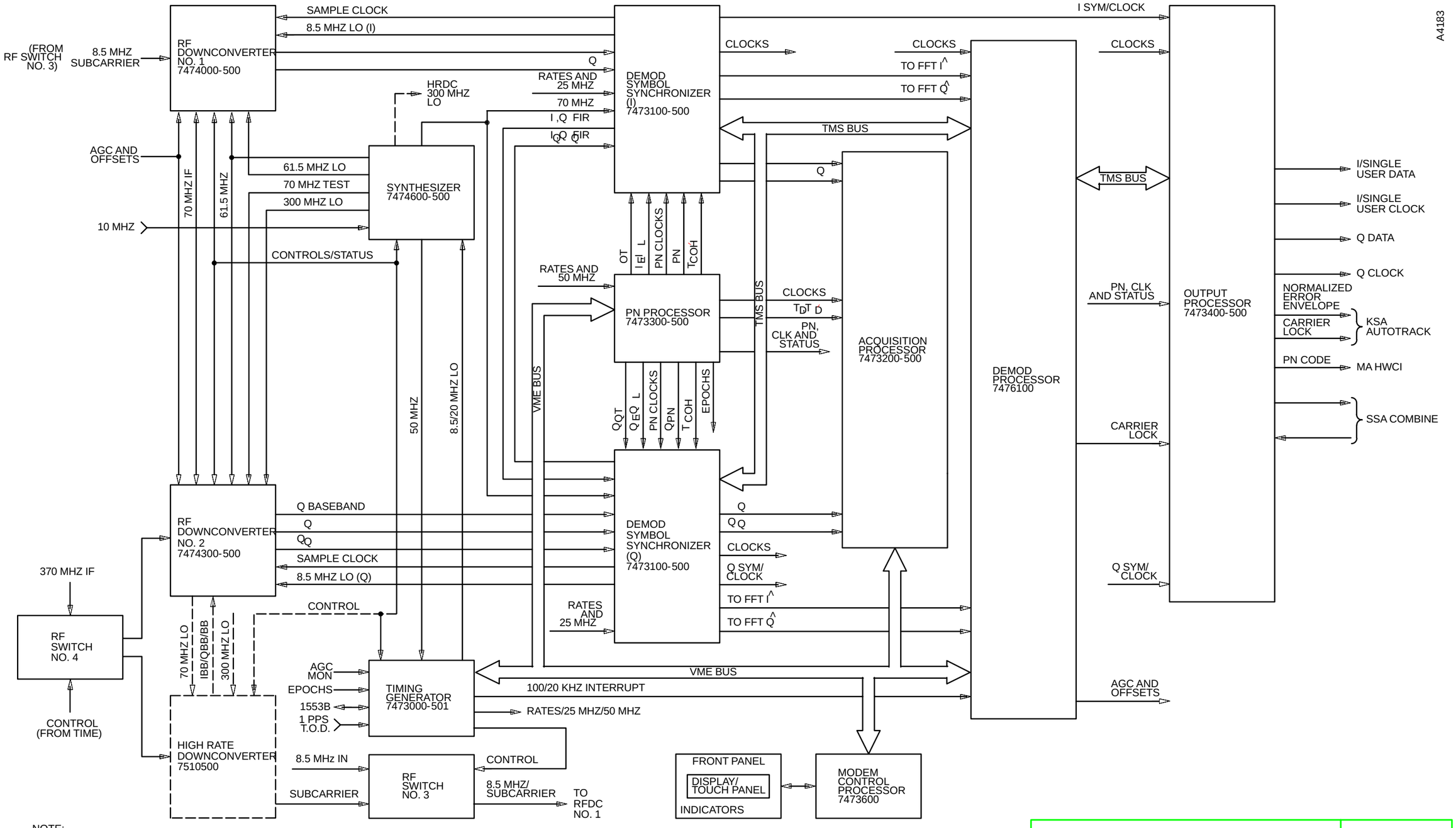
b. PN Controller Function. The PN controller function controls all aspects of the PNP and ACQR operation. Upon a Demod Configuration command, the ACQR and PNP configurations are updated (this is only utilized in the spread mode). Next, PN acquisition is started upon receipt of a Start Acquisition command. During the PN acquisition, this function searches the range of code and Doppler uncertainty and provides code offsets and Doppler estimates to the DMDP. The PN acquisition is performed in parallel with the DMDP's carrier acquisition process until the DMDP indicates frequency lock.

   Upon frequency lock, this function indicates PN lock and begins to update the open code loop until a timeout occurs, at which time it will transition to track; otherwise, the search process continues. The open loop track process uses the Doppler value that was found during the DMDP's FFT search to update the track code NCO. Once processing transitions to track, the code loop is aided with the DMDP's carrier Doppler, TDRSS Doppler, and return compensation values. The reacquire PN code function becomes enabled when the phaselock status received from the DMDP indicates no phase lock. During PN reacquisition, the logic searches a range based on time-of-day, the estimated time bias, and the ephemeris uncertainty and processing reverts to that point leading up to the DMDP initiating a frequency loss of lock.

c. Demod Controller Function. The Demod controller function controls all data transfers between the MCP and DMDP. This function sends a Perform DC Bias command to initialize DMDP to a known state and verifies the DMDP's operating mode status as standby. All commands to the DMDP are sent asynchronously with a semaphore scheme that allows only one command to be processed at a time. Next, the DMDP is configured.

   During carrier acquisition, DMDP interrupts MCP when the carrier has been acquired. Once every ten milliseconds, DMDP sends its status to MCP. All lock bits are monitored for lock during the entire one second period and if any ten millisecond status report shows a loss of lock, that entire one second period is reported as no lock. This function also resolves channel ambiguity.

d. Tracking Services Function. This function processes the raw measurements into the desired user outputs. All tracking services functions are performed every second once the IR has entered the track operation mode. Update Doppler measurements is performed in all modes. Update range measurements and update time transfer measurement is performed in data group 1, modes 1 and 3.



NOTE:

1. FREQUENCIES FOLLOWED BY LO ARE CONTROLLED BY NCO'S LOCATED ON THE VME OR TMS BUS.
2. DASHED LINES INDICATE KSA MODIFICATION KIT.

FIGURE 4-1. INTEGRATED RECEIVER FUNCTIONAL BLOCK DIAGRAM

e. Time Management Function. This function maintains time-of-year (TOY) and various timers (phase-lock timer, acquisition timer, and epoch measurement timer) that are used throughout the IR. The TOY, maintained by the TIME PWA, is updated once a second with a resolution of one millisecond. The phase-lock time is zeroed upon receipt of Carrier Frequency Acquisition event and incremented until the DMDP enters carrier phase lock with a resolution of ten milliseconds. The acquisition timer is zeroed upon receipt of a Start Acquisition command and is incremented with a ten millisecond resolution until the applicable lock is achieved, based on mode. The update epoch measurement reads the first two epoch measurements following the 1-PPS Interrupt event.

f. Interactive Touch Panel Controller Function. This function processes the touch panel entries received from the display and updates the display based on those entries.

g. Performance Monitor Function. This function consists of the online BIT, extended BIT, confidence BIT, manage fault light, and prepare status reports. Refer to section 3 for explanations of BITs and manage fault light functions. The prepare status reports function examines status and data from all major data sources and converts the information into the appropriate status report format. All reports are available to be read by the 1553 bus interface at the 300 millisecond mark after each 1 PPS. The reports consist of the following: demodulator configuration report, demodulator performance report, extended BIT report, and tracking services report.

h. Ephemeris Processing Function. This function is made up of the following subfunctions: model forward state, return Doppler compensation, estimate ephemeris time bias, and calculate Doppler uncertainty. The model forward state function calculates the forward code state based on the current ephemeris data every two milliseconds. It also models the forward carrier based on the current ephemeris data every half-second. It starts to model the forward PN code state when the TOY equals the service start time. The output of this function is used in the select search interval function and the tracking services function. The return Doppler compensation function performs Doppler pre-correction on the return signal by controlling the TIME NCO. It also performs Doppler control and frequency sweep based on ADPE commands. The NCO is updated every two milliseconds based on a linear interpolation of the ephemeris half-second points.

4-3.3 DMDP Program

The DMDP program provides frequency acquisition, data tracking, and real-time demodulator control in the IR. The DMDP is under the control of the MCP program but the actual processing flow is a function of external inputs from the peripheral hardware. The DMDP program receives command and configuration data from the MCP and DMDP processing status is sent to the MCP. The DMDP program is comprised of the following functions:

a. Interpret Commands. The MCP to DMDP interface uses a semaphore scheme that allows only one command to be processed at a time. The DMDP program notifies the MCP when it has finished processing a command. Valid commands are passed on to the system. Invalid commands are ignored. The possible commands are: reset TMS, perform dc bias, BIT, configure, start acquisition, Doppler estimate, and initialize.

b. Configure Demodulator. This process, upon power-up reset, will: copy the firmware program from PROM to RAM, set up the configuration data area to a known default configuration, and proceed with the configuration process. For a configuration command, this function sets up the firmware and hardware as per the configuration data which is either: the default configuration or downloaded initial configuration command data from the MCP (the MCP also downloads auxiliary configuration data for use in subsequent processing stages). Complete configuration is performed within 20 milliseconds.

c. Signal Processing. This function provides the frequency acquisition and data tracking capabilities for the TMS. This function includes the following subfunctions: acquire the carrier, track the carrier, noncoherent AGC, coherent AGC, compile the DMDP status, track the data, update configuration, and estimate RMS noise. The acquire-the- carrier function provides for FFT processing to search for the carrier over a range of Doppler uncertainty. Track the carrier provides the phase-lock loop tracking function for carrier, subcarrier, and recovered carrier. Noncoherent AGC provides carrier lock status based on the input signal power and the phase error. Both lock and loss of lock conditions are monitored. Coherent AGC adjusts and maintains constant signal levels to the decoder and carrier loop functions to optimize their performance. The AGC value is based upon the measured signal magnitude.

   Compile DMDP status function utilizes the semaphore scheme whereby the TMS is allowed to run without queuing up its status data. If TMS has determined that the MCP has not completed its access of the status data then no new status data is written to the interface. Each time the TMS updates status, it increments a counter that is part of that status. The counter allows the MCP to affirm that status is new, but static. Track the data function monitors the hardware and carrier lock status, keeping track of the data tracking peripherals and monitoring for both a lock condition and a loss of lock condition. Update configuration provides updated modifications to the demodulator configuration during the processing of a signal. Estimate RMS noise computes an estimate of the RMS noise level for the soft decision circuitry based upon a lookup table.

d. Commanded BIT. Commanded BIT results from the direct command from the MCP and provides status back to MCP. This BIT supports the following tests: self-contained ASIC BIT and bidirectional memory test of dual port RAM in concurrence with the MCP. Refer to section 3 for further information on these tests.

4-4 States Of Operation

4-4.1 Operating States Introduction

4-4.1.1 The IR operating states consist of the return service states which include a forward model. The return service states relate to the overall receiver operation of the IR; while the forward model relates to the Modulator/Doppler Predictor (MDP) parameters and commands necessary for coherent service tracking. The MDP is a unit within the forward service (uplink) USS equipment. The parameters used by the forward model are: IF offset frequency, translation frequency, PN modulation configuration, and the Doppler configuration. The IR forward model and the return states are independent, with the forward model reflecting the state of operation of the MDP. The forward model and return states share two common states, confidence test in progress and extended BIT. The following paragraphs describe the necessary steps to configure the forward model and for the return states to reach the track state.

4-4.1.2 The confidence test in progress state is entered at power-up or reset and the TEST LED is turned on. During this state, the IR executes its confidence BIT test and does not respond to any 1553 bus communications. This state completes in less than 10 seconds and the TEST LED is turned off. If the confidence BIT fails, the FAULT LED is turned on and remains on. The extended BIT state is entered by an Extended BIT command over the 1553 bus (remote control) or front-panel display initiation (local control) and exits upon completion or by termination of BIT by either front panel or 1553 bus command.

4-4.2 Forward Model

4-4.2.1 Refer to figure 4-2 for the following discussion. Forward model standby is entered by the forward model at the completion of the confident BIT test or by command via the 1553 bus interface. Forward model standby indicates that the IR forward model is ready to receive a Common Configuration command. This command contains configuration parameters which are common and require time synchronization with the

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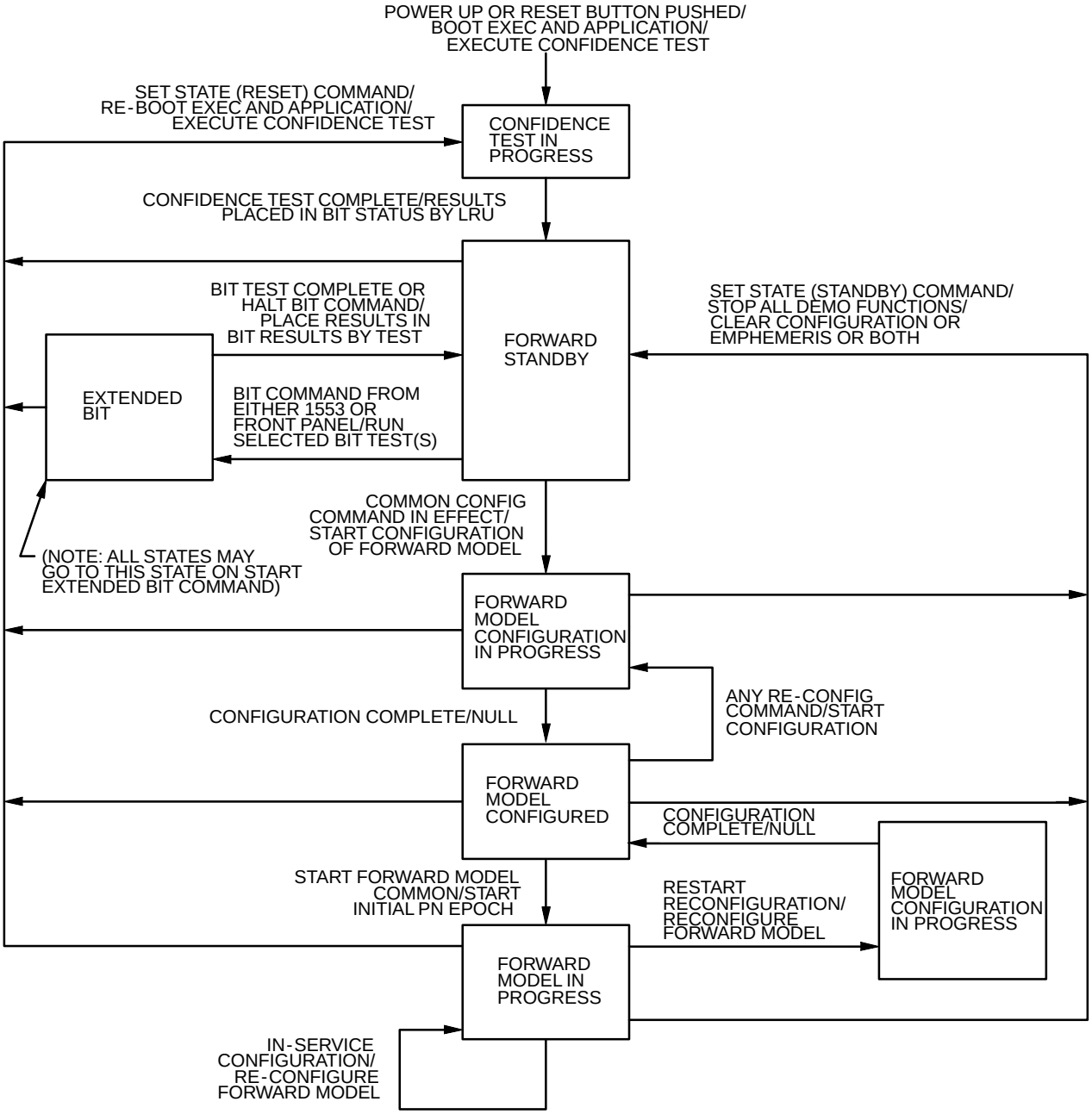


Figure 4—2. Forward States

MDP. These parameters are used to setup the forward model. Once the Common Configuration command is accepted, forward model configuration in progress is entered. This indicates that the IR forward model is dedicated to the specified forward model configuration. Once the IR forward model is configured, forward model configured is reached.

4-4.2.2 Forward model configured indicates that the IR has configured itself to the specified Common Configuration command and is awaiting a Start Forward Model command or a Forward Model Cold Start command. The Start Forward Model command allows the IR to transition to forward model in progress. The Forward Model Cold Start command is used when the startup of the IR cannot be synchronized with the startup of the MDP due to certain operational scenarios. The Cold Start command contains information on the PN state of the MDP at a specified time. The IR propagates this state to start the forward model at that specified time and then the IR enters forward model in progress.

4-4.2.3 Forward model in progress indicates that the forward model has started. For coherent services, this state must be active prior to the IR return state entering acquisition in order to meet acquisition and tracking requirements. While forward model in progress is active, the IR accepts the following MDP commands for coherent service; frequency sweep, Doppler control, and break lock. The frequency sweep is used to assist in forward user acquisition if the user state vector is suspect or the transponder receiver “best lock” frequency is suspect. The Doppler control provides the Doppler compensation control information that is sent to the MDP. Break lock notifies the IR that the MDP is performing a forward break lock so that it may be simulated in the forward model.

4-4.3 Return States

4-4.3.1 Refer to figure 4-3 for the following discussion. The standby state is entered at completion of the confidence BIT test or by command via the 1553 bus interface. The standby state indicates that the IR is ready to receive a Specific Configuration command. This command contains configuration parameters that are specific to the IR (not common or synchronous to the MDP or PTE). Once the Specific Configuration command is accepted, the IR starts configuration of the unit, excluding the forward model. When the configuration process begins, the IR enters the configuration in progress state. This state indicates that the IR is dedicated to the specified configuration. No other signal acquisition or tracking is done while in this state. At the completion of the configuration process, the IR transitions to the configured state.

4-4.3.2 The configured state indicates that the IR has configured itself to the specified Specific Configuration command and is ready to start the acquisition and tracking of the specified signal. The acquisition state indicates that the IR is attempting to acquire the signal as configured. Any Reconfiguration command during this state transitions the unit to the configuration in progress state. Upon receipt of a PN/carrier lock, the IR transitions to the tracking state. The tracking state indicates that the IR has achieved lock, and is tracking the signal as configured. This is the only state in which the tracking report data is valid. The IR stays in this state until either loss of lock or a command requiring a state change is received. Upon loss of PN/carrier lock, the IR transitions to the reacquisition state. The reacquisition state indicates that the IR is attempting to reacquire the signal based on previous Doppler and range information achieved during track. The IR stays in this state until either lock of PN/carrier is achieved or a command requiring a state change is received.

4-5 Carrier Acquisition and Tracking

4-5.1 The IR incorporates a dual-channel demodulator structure to provide the necessary tracking performance for all SSA and MA and supported KSA return service modes. A dual-channel demodulator structure is ideal for all waveform types but is designed primarily to provide nearly optimum tracking of unbalanced power and/or symbol rate modes (unbalanced quadrature phase-shift keyed (UQPSK)). Staggered QPSK (SQPSK), QPSK, and binary PSK (BPSK) signals are all special cases of the UQPSK format such that the receiver can be

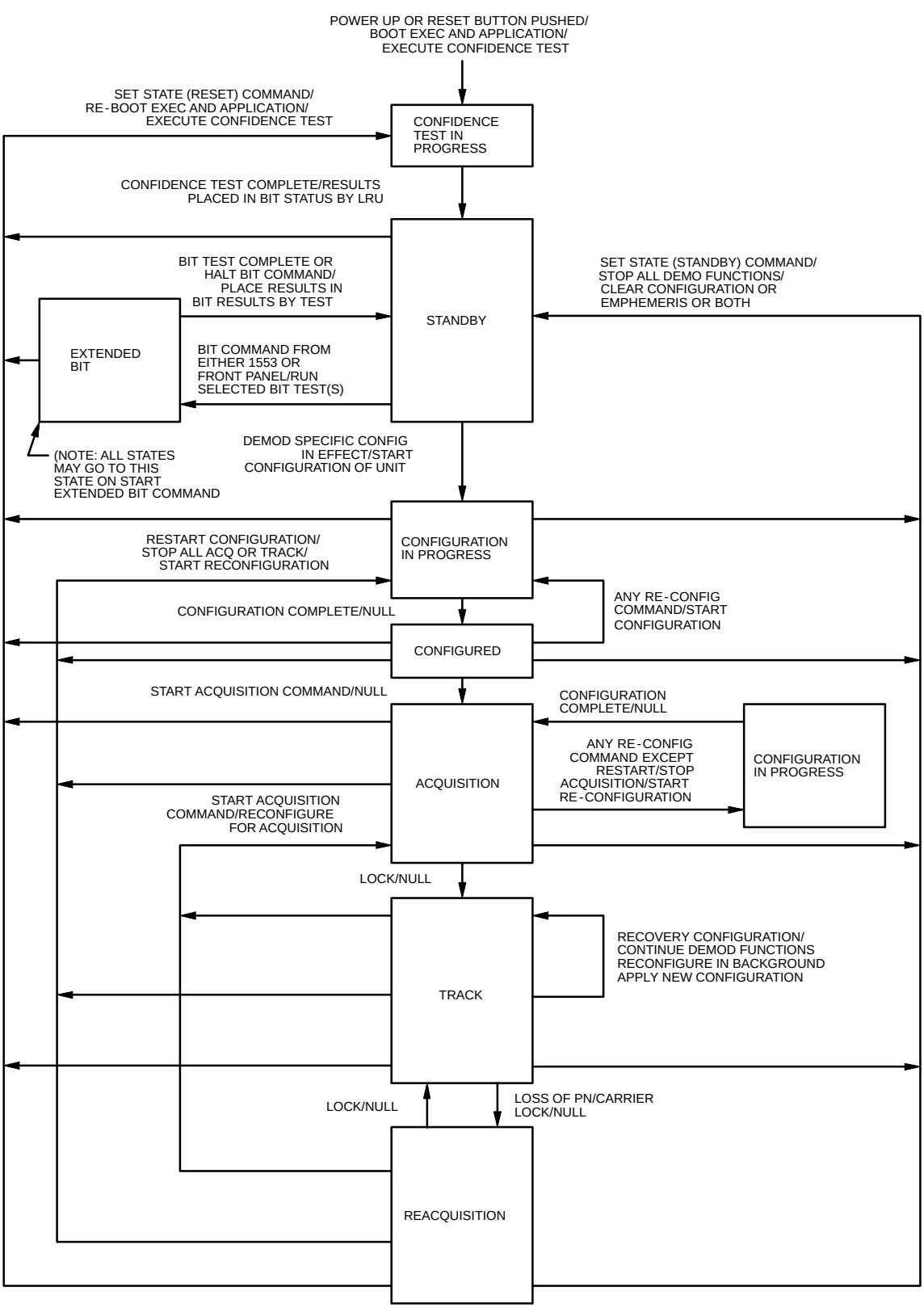


Figure 4—3. Return States

configured for any mode with only minor changes of timing signals. The dual-channel demodulator architecture is shown in figure 4-4.

4-5.2 The demodulator consists of two identically structured, single-channel carrier tracking loops to demodulate the inphase (I) and quadrature (Q) signal components. The received I and Q waveform sets are despread using multiplication techniques with the appropriate I and Q channel reference code prior to integrate-and-dump filtering. For nonspread modes, the code reference is set to all one's. In addition, the reference code pulse shape matches the channel symbol type (NRZ or biphase). Through biphase half-symbol inversion, biphase symbol formats are effectively removed prior to the matched filters, simplifying carrier and PN loop operation.

4-5.3 The received I and Q channels are processed separately, with the I_I and Q_I integrate-and-dump (I/D) filters matched to the I data symbol rate and the I_Q and Q_Q I/D filters matched to the Q data symbol rate. Each carrier loop receives timing information for the I/D filters from its corresponding integrated symbol synchronizer loop. Each carrier loop independently computes and filters its phase error measurement, where the phase measurement is made using a decision-directed phase detector. The demodulator then weights the I and Q channel accumulated phase error terms relative to the ratio of the two-channel symbol rates and power imbalance and then sums the two weighted error terms to create a final error term into the loop filter. This minimizes the magnitude of the resultant crosstalk terms and maximizes the signal-to-noise ratio (SNR) into the carrier loop filter.

4-5.4 The phase measurement weighting, final phase error generation and the loop filtering functions are performed in firmware. This provides ease of bandwidth change as the data rate varies and allows variation in the filter order between acquisition and track modes. The loop filter output is then applied to a numerically controlled oscillator (NCO), which subsequently controls the phase of a digital phase rotator. The loop filter and NCO control are updated at the lower channel symbol rate, in general, with a minimum sampling rate on the order of 800 symbols per second (sps).

4-5.5 The IR allows carrier acquisition to be performed in parallel with PN code acquisition for data group (DG)-1 mode 3, since the carrier loop can acquire on the nonspread Q-channel while the PN code is acquired on the spread I channel. In addition, the highly flexible nature of the receiver allows independent operation of two parallel carrier tracking loops. In particular, for KSHR mode 1, the IR simultaneously demodulates the recovered subcarrier provided by the high-rate down converter (HRDC) using the I-channel carrier loop, and provides Doppler tracking support by tracking the HRDC-recovered carrier using the Q-channel carrier loop in a phase-lock-loop mode.

4-5.6 A key feature of the carrier acquisition process is the use of a flexible discrete fast fourier transform (FFT) element within the carrier phase detector. This FFT, in conjunction with the dual-channel carrier recovery, provides fast-acquisition capabilities while eliminating carrier false lock concerns. The FFT operates coherently over the frequency estimation period to provide frequency error estimation capabilities even with minimum carrier-to-noise ratio (C/No) conditions. With frequency acquisition performed primarily by the FFT, the carrier loop needs only to perform lock-in, resulting in fast and predictable acquisition performance. During acquisition, the carrier loop operates as a first-order loop to provide fast lock-in while minimizing transient effects. Once acquisition is detected, the loop switches to a third-order loop structure to provide tracking capabilities even for worst-case dynamics.

4-6 PN Acquisition and Tracking

4-6.1 To achieve PN code acquisition at all data rates, the IR utilizes two 4-to-1024 tap 2-bit correlators (per channel) operating in parallel. This provides the required acquisition capabilities under all conditions, even with Manchester coding at 1000 sps in DG-1 mode 3, which is the most difficult acquisition mode. A 1024 FFT is included in the process to provide a significant speed/performance improvement through the use of parallel Doppler-bin processing. Correlation is performed

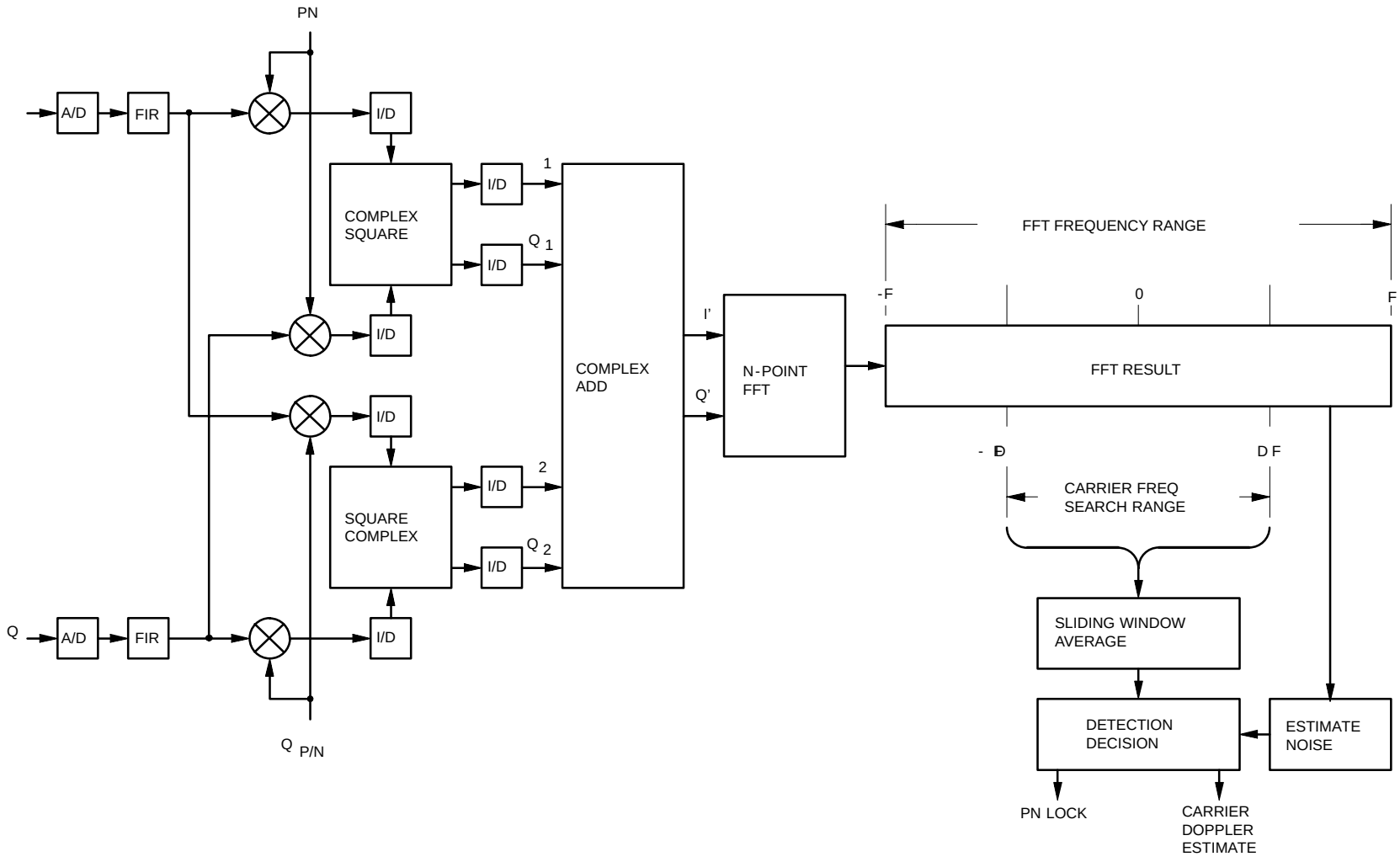


Figure 4—4. Carrier Acquisition Functional Block Diagram

using 2 bits only from the I/Q finite impulse response (FIR) signals with the MCP controlled replica codes. The replica codes are controlled by the MCP and generated by PNP.

4-6.2 The code correlation process takes place in the DMSSs with their outputs (I/Q acquisition signals) sent to the MCP-controlled ACQR. ACQR is configured for coherent and noncoherent correlator combines. Coherent combining is used to increase the correlator gain and reduce random noise whereas noncoherent combining is used to increase the gain at the magnitude detector output. Dwell timing/correlator taps are configured as per the dwell period to be used. The dwell period is based on the code uncertainty, symbol format, symbol rate, and PN chip rate. The code uncertainty is based on the ephemeris data. Once the dwell period is determined, the PNP cascade counters are set (T'coh, Tcoh, Td', and Td).

4-6.3 During PN code acquisition, the MCP controls the search over the range of code and Doppler uncertainty and provides code offsets and Doppler estimates to the DMDP. The search interval function is performed by updating the PN code state and NCOs to search the code and Doppler uncertainty based upon the mode. Next, code offset is computed by determining a code offset calculation every peak detect interrupt event. PN code acquisition does not transition to PN tracking until carrier frequency acquisition occurs. For the DMDP to verify the presence of a carrier signal, the signal must be despread and supplied the starting carrier Doppler frequency for the DMDP's search interval (for spread modes only). The despreading is done by using the calculated code offset to update the TRK PN code generator. The code Doppler value that was used at the start of this search interval is used to set the frequency of the TRK code NCO. The corresponding carrier Doppler value is passed on to the DMDP. This initiates the DMDP to do an FFT search over the search interval (see figure 4-4). Once carrier frequency acquisition has been achieved, PN code acquisition transitions to PN track.

4-6.4 PN code tracking is performed using a coherent delay-lock loop PN code tracking process (see figure 4-5). Once tracking mode is achieved, the code loop is aided with the DMDP's measured carrier Doppler, TDRS Doppler, and receive compensation values. The TRK code NCO is updated every 10 milliseconds using a second-order tracking loop with the loop coefficients supporting a 0.5-Hz loop bandwidth to provide good noise characteristics and to minimize peak bias errors during high dynamics conditions. The loop tracks the higher power Q-channel for DG-1 modes 1 and 2, and is automatically reconfigured to allow tracking on the I-channel for DG-1 mode 3.

4-7 Symbol Synchronization

4-7.1 The IR incorporates a pair of independent symbol synchronizers, one each for the I and Q data channels. Each synchronizer loop is a flexible structure easily adjusted to match received symbol format, anticipated symbol energy to noise ratio (Es/No), symbol jitter through phase detector reconfigurations, and for control of the synchronizer loop bandwidth.

4-7.2 The decision-directed symbol synchronizer is inherently capable of providing the required synchronization capabilities for both NRZ and biphase symbol formats. This synchronizer is decision-directed in that the polarity of the timing estimate out of the timing I/D filter is dependent upon the polarity of the data decision. For a symbol synchronizer, timing information is available given only that there was in fact a data transition. The decision-directed synchronizer continually monitors for transitions and updates the loop only when one is detected. This provides optimum performance even as the transition density decreases or long periods of no transitions are encountered.

4-7.3 The symbol timing phase-error detector is optimally reconfigured to match the received symbol format, either NRZ or biphase. The loop filter bandwidth is varied to best match the anticipated received symbol jitter and Es/No. For biphase symbols, the synchronizer performs integrations every half bit, the first centered over the first transition with the second around the middle transition. The decision-directed synchronizer takes advantage of derived knowledge of the biphase waveform to provide excellent tracking

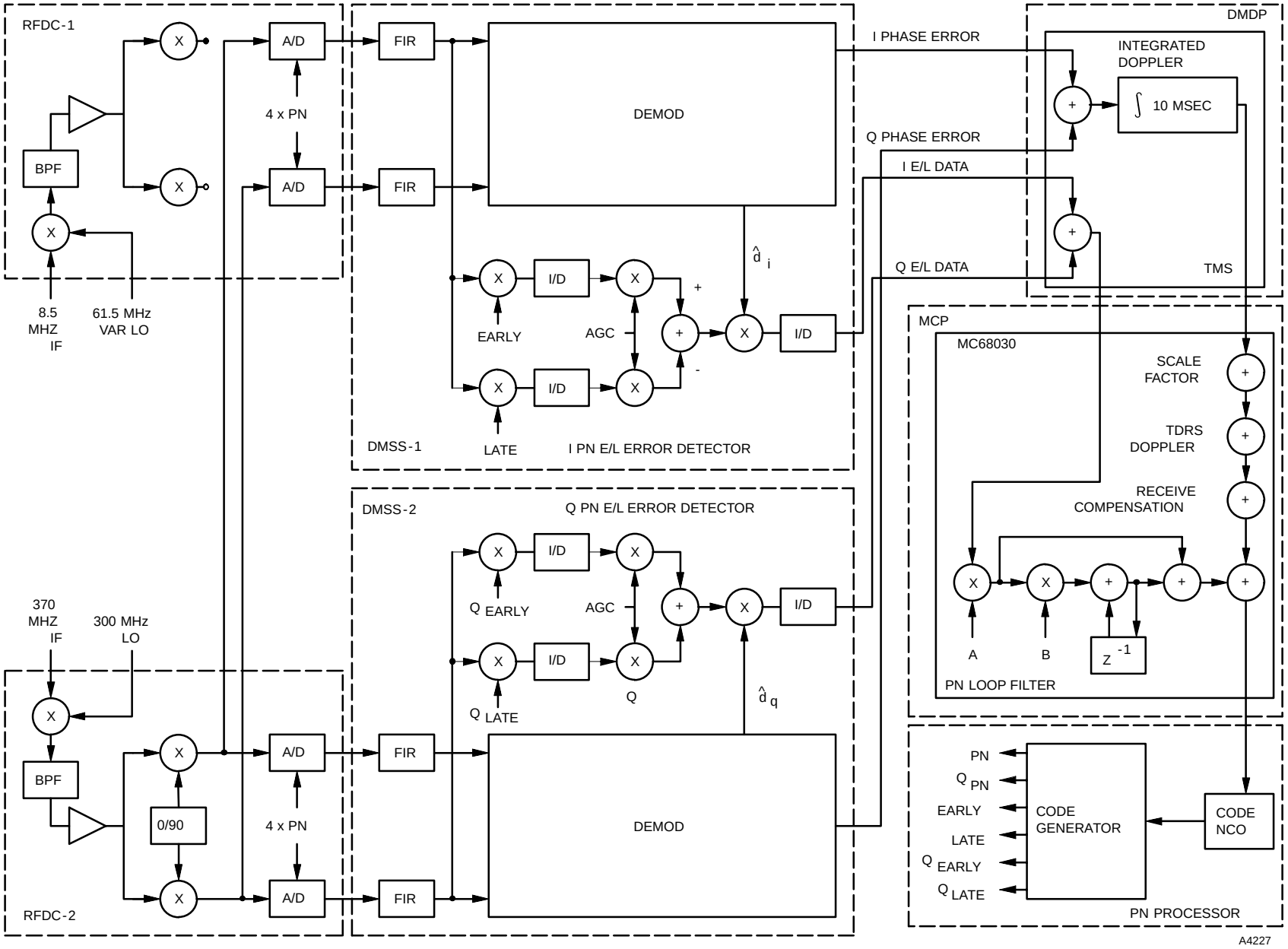


Figure 4—5. PN Tracking Functional Diagram

characteristics with biphase data. Since there is always a mid-symbol transition with biphase symbols, the mid-symbol I/D result is always applied to the loop. The start of symbol integration is applied only when a transition is detected, per the case of NRZ symbols.

4-7.4 For NRZ symbols during acquisition, the synchronizer integrates over a full window to cover the full timing uncertainty. During tracking, however, the synchronizer narrows the timing integration window down to provide superior noise performance/tracking capability. This is achieved given the dual set of integrations required to optimally synchronize to biphase symbols.

4-7.5 The timing loop filter drives a direct-sine NCO that functions as the primary clock source for the channel. This provides continuous timing adjustment capabilities for all modes. The NCO output is converted up to a 12-MHz-to-24-MHz frequency range to allow generation of all channel-dependent clocks from this one source. For DG-2 and Shuttle modes, the upconverted NCO output is applied directly to the appropriate input ADCs as the sample clock, and are divided down to create all necessary symbol rate clocks. For DG-1 modes, the A/D output is sampled relative to the PN code rate although all symbol rate-dependent sample clocks are derived in accordance with DG-2 modes.

4-8 AGC

4-8.1 The IR includes two independent data AGC loops with separate control to provide consistent soft-decision levels for both the I and Q data channels. The noncoherent AGC attempts to maintain a constant signal-plus-noise level for the analog input signal going to the ADCs in the RFDC. The coherent AGC adjusts and maintains a constant signal level to the decoder and carrier loop functions to optimize their performance. As shown in figure 4-6, digital scaling is employed to guarantee uniform performance of all loops. Being digital in nature, the gain in all applicable processing paths (carrier, symbol synchronizer, and PN tracking loops) is identical.

4-8.2 The Viterbi decoding algorithm is relatively insensitive to gain variation or equivalently, soft-decision threshold errors. Thus, operation over a relatively wide dynamic range is possible with a noncoherent AGC with minor impact to BER performance. The AGC's operating point is optimized for 10^{-5} decoded BER performance. A first-order AGC loop is used with a bandwidth less than 1 Hz to minimize its effect on carrier and PN tracking loops. This bandwidth is sufficient to allow good tracking during worst case specified fade conditions.

4-9 SSA Combining

4-9.1 The IR supports two combining modes corresponding to DG-1 synchronous, identical data modes, and SSA combining where the recovered data from two SSA service chains (SSA-1R and SSA-2R) must be combined prior to the decoder. For DG-1 modes, the combining is provided as a predetect function internal to the demodulators matched filter structure, providing a 3-dB signal-to-noise ratio into the carrier and symbol tracking loops.

4-9.2 SSA combining is performed as a postdetect function. Any SSA-IR is capable of functioning as the combiner/data detector unit. Combining is always performed after the deinterleaving process. Figure 4-7 shows the functional implementation of the SSA combiner performed by the OUTP. The IR monitors both the internal input symbol stream, the external input stream, and the sum stream to determine; (1) if a 1/0 ambiguity condition exists, and (2) if the internal/external input channels are usable. Through continuous monitoring, the IR provides some protection against degraded operation, due to either a short-term loss-of-lock condition, or signal fading in one channel only.

4-9.3 Efficient combining requires a minimum of 5 bits from each source. In addition, synchronization requires coarse knowledge of transit delay difference to guarantee time alignment. Timing error may be due to either unaccounted differences in the two-channel path delays and/or symbol synchronizer effects. Channel delays may be measured to reasonable accuracy and

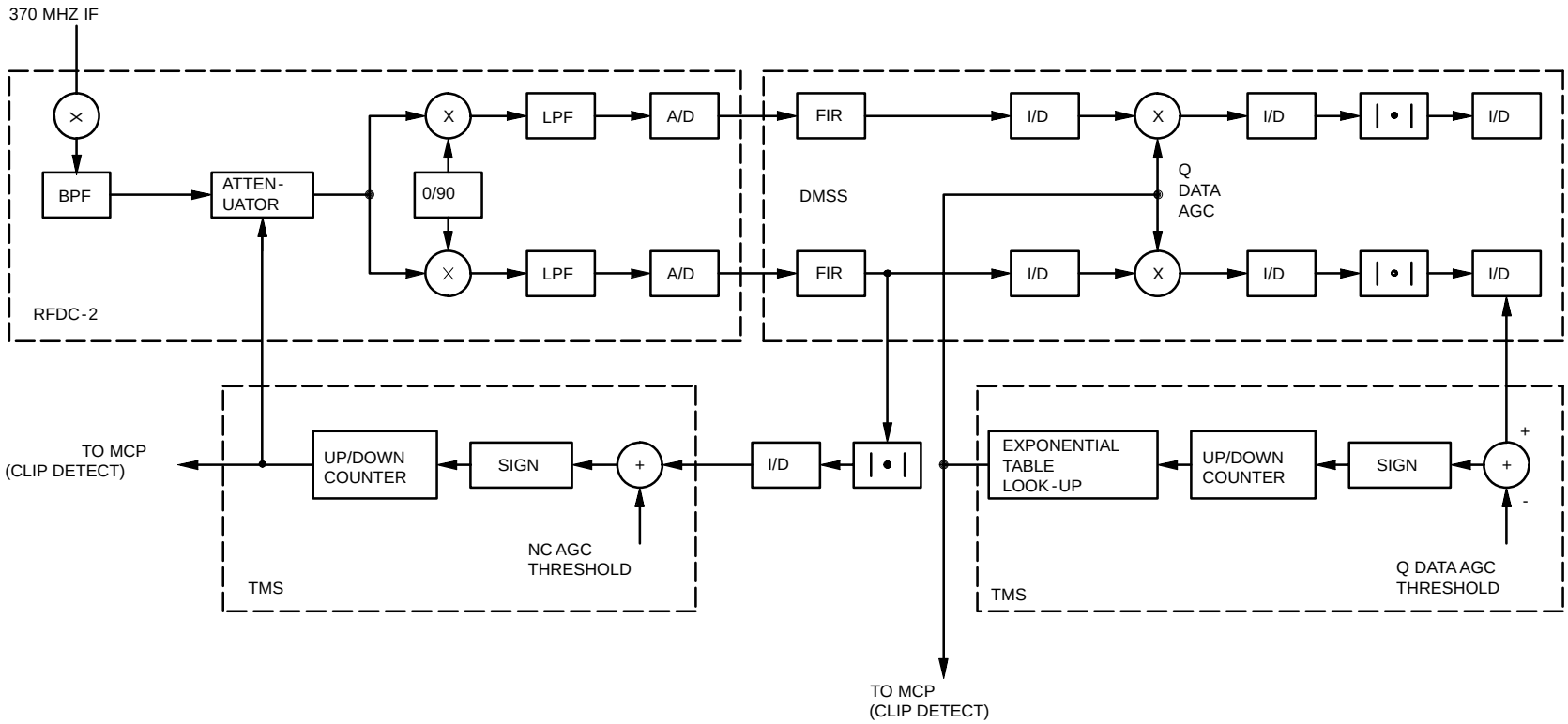


Figure 4-6. Coherent/Non-Coherent AGC

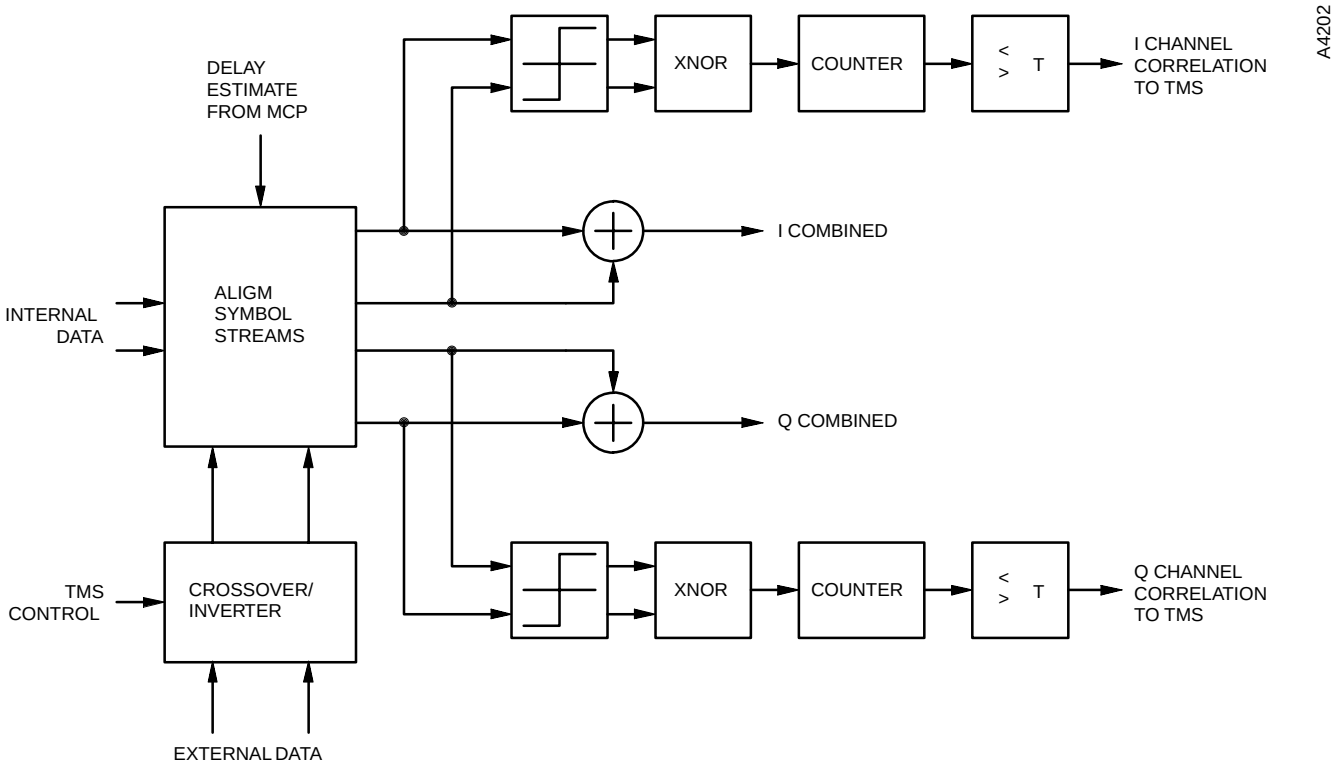


Figure 4—7. SSA Combining Functional Diagram

removed through the incorporation of a variable delay (system must store all potential receiver combinations and associated delay values). Of much greater concern is timing error due to symbol synchronizer output timing jitter. To avoid excessive degradation in a combining mode, combining is utilized only on channels whose symbol jitter is much less than 0.1 percent. In so doing, the symbol synchronizer loop bandwidth may be narrowed considerably both to guarantee better slip performance and to maintain much more stable clocks.

4-10 Ambiguity Resolution

Channel ambiguity does not apply to DG-1 modes or BPSK modes. Channel ambiguity is resolved for the DG-2 UQPSK modes and KSHR mode if at least one of the following conditions exist: I/Q power ratio is 4:1, only one of the two channels is coded or the channels use different codes, or symbol rates differ by more than 25 percent. Channel ambiguity is also resolved for the DG-2 SQPSK alternate symbol modes.

4-11 Ephemeris Processing and Tracking Services

4-11.1 Ephemeris processing maintains an ephemeris database with a maximum size of 50 minutes worth of data. The IR is capable of saving ephemeris updates up to 60 minutes past its current time. Any ephemeris data greater than 60 minutes in the future is discarded. Ephemeris data provides for compensation of the carrier and code (see figure 4-8).

4-11.2 Range, Doppler, and time transfer measurements are all made as a byproduct of the implementation of the carrier and code tracking loops in the IR. The tracking loops operate in the

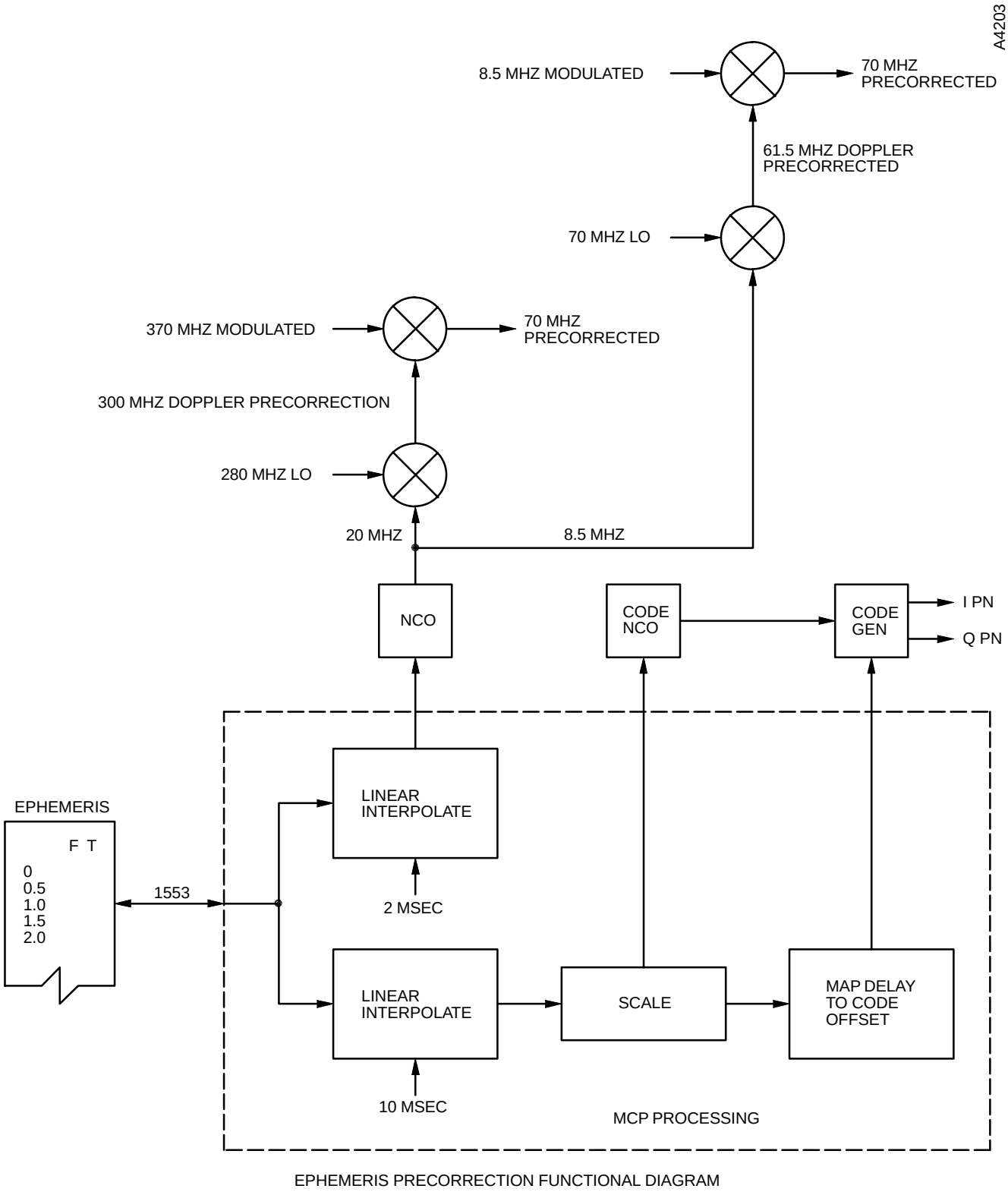


Figure 4—8. Ephemeris Precorrection Functional Diagram

closed-loop fashion of error detection, filtering the error, and using those to generate a replica of the input signal, which is beat against the input, and so on. Clearly, if the loop is perfectly locked to the input, then the replica has the same frequency and phase characteristics as the input.

4-11.3 In the IR there are two loops, a code tracking loop inside the carrier tracking loop. After lock is achieved, the error signals represent carrier and code phase offset and are generated from the carrier phase detector and the PN early/late detector. The carrier and code loop NCOs are used as the primary point of control after the process is initialized by setting the code generator phase and zeroing of the NCO accumulators. NCO updates are loaded into the control register nominally at a 1-kHz rate for the code loop and between an 800-Hz and 20-kHz rate (variable as a function of data rate) for the carrier loop. The system strobe is synthesized from the precision 10-MHz input, thereby ensuring that the period over which a control word controls the NCO is precisely known. The NCO control word actually represents phase rate. Since the maximum count of the accumulator represents one cycle out of the NCO, the control word is scaled as the phase changes over each update period of the update strobe, with the resolution of each update controlled by the size of the accumulator. For STGT, 24-bit accumulator NCOs are used resulting in a phase update as small as 0.3745 microradians per update clock. The update strobe must be at least twice as fast as the highest Doppler offset the loop is required to track.

4-11.4 The IR is designed to cover the entire S-band range using only the NCO in the carrier tracking loop, since the input “coarse NCO” which does the down conversion from 370 MHz to 70 MHz is used to make Doppler correction only for K-band service. (This is also driven by MA, since the coarse NCO is not in the MA signal path.) The maximum S-band Doppler, assuming 15 km/sec velocity, is 115 kHz. Over a system strobe period, the NCO phase may then change as little as 4.49 microradians, or as much as 115 cycles. This is important because due to the precision intervals over which the control words and strobes operate, it is sufficient to know what control words were applied to the NCO to know precisely the output of the NCO and the internal phase of the NCO. Since the NCO output is the replica of the input signal, the IR knows the characteristics of the input signal automatically as a byproduct of locking to the carrier and PN code, functions that are required even if no tracking services were required.

4-11.5 The noise performance of the loops is a function of the averaging interval, the loop bandwidth, the C/No into the loop, and the noise characteristics of the loop types. Based upon a 1-second average period, the IR generates range and time transfer measurements with a standard deviation of only 2 nanoseconds at a very conservative worst-case C/No of 26.9 dB-Hz. In addition, specified range-rate measurement accuracy is met for all symbol rates under free flight and powered flight dynamics.

4-12 Modem Control Processor

Refer to figure 4-9 for the following MCP functional description. MCP consists of a 25-MHz 68030 processor based VME bus controller, 1 Mbyte zero-wait state static RAM, four EPROM sockets (27C010 EPROMs = 512 kbytes), two serial channels (68561 based) - up to 38.4 kbaud (RS-232 compatible, one channel selectable RS-232/RS-422/RS-485), and two 24-bit timers. The MCP address select enables the control logic section of the slave boards on the VMEbus by matching address lines A23-A19 with the board select bits of the P2 connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the transfer function to be processed.

4-12.1 68030 Microprocessor

4-12.1.1 The 68030 contains sixteen 32-bit general-purpose address and data registers, two 32-bit supervisor pointers, and one user stack pointer. The non-multiplexed address and data bus can be used in an asynchronous mode to allow optimized hardware interfacing to the buses. Synchronous bus cycles are also supported by the 68030 to accelerate transfers. To offer high data throughput in conjunction to the static RAM, a 16-MHz CPU clock frequency is provided. The

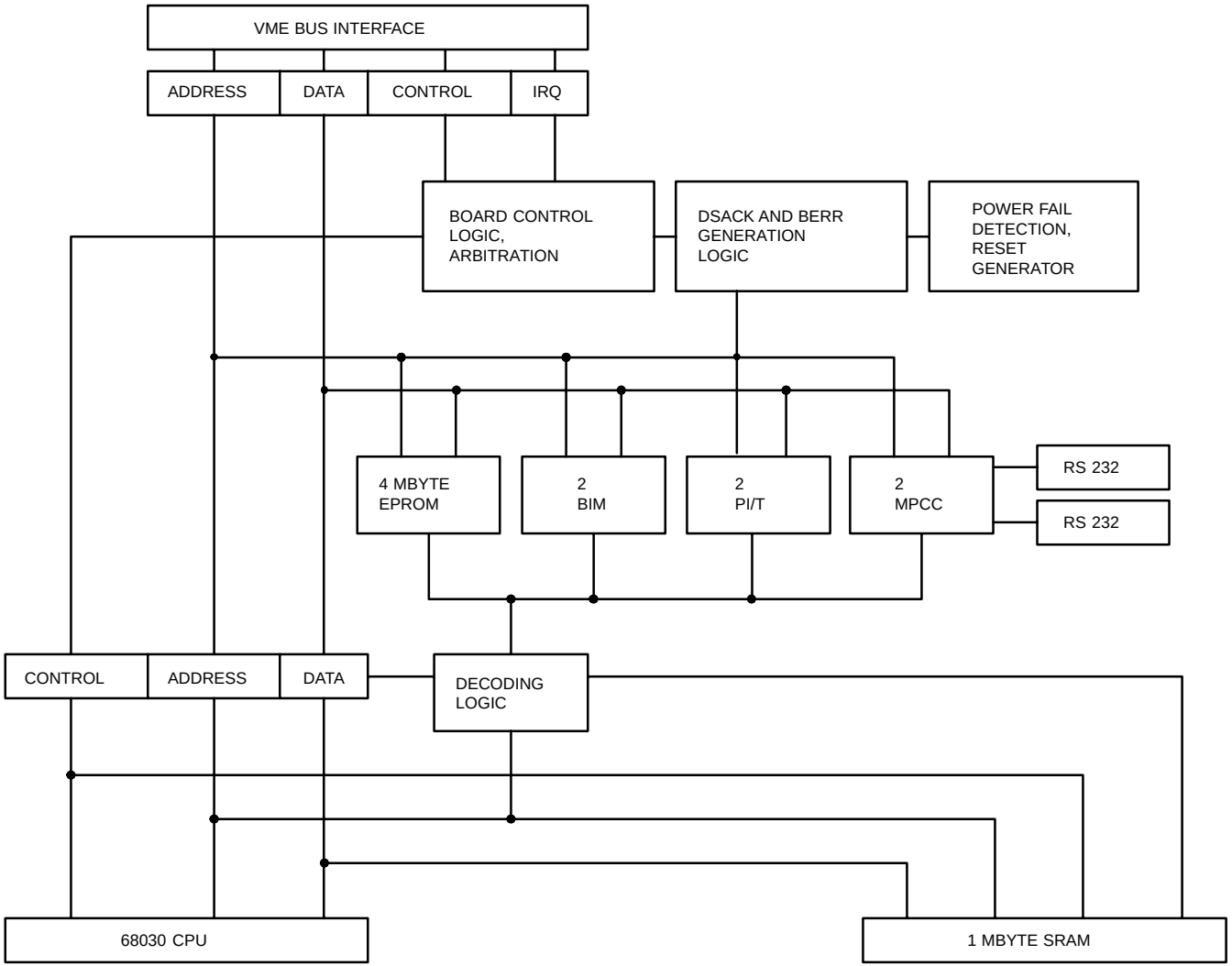


Figure 4—9. MCP Functional Block Diagram

256-byte on-chip data and instruction caches provide a maximum computing rate of 8 MIPS by unloading the system buses from opcode/program fetches.

4-12.1.2 The data bus interface of the 68030 is very flexible and provides a dynamic bus sizing where the data bus size can be adapted. This feature allows the interfacing of 8-, 16-, or 32-bit organized memory and/or I/O devices. For easy exception handling and recover of bus errors, the 68030 stores all internal states in the stack. The MCP contains a local bus interface (LBI). The following devices are connected to the LBI: local SRAM, EPROM, serial I/O controllers (2), parallel interface and timers chips (2), and local interrupt handler chips (2).

4-12.2 EPROM and SRAM

The first two read cycles after a reset of the 68030 processor are fetches of the initial interrupt stack pointer and the initial program counter. These cycles are executed under addresses $0 and $4, respectively. A special control logic maps the EPROM down to this address to start the CPU out of the installed EPROMs. The EPROM area is 32 bits wide, offering maximum throughput for the programs running in the EPROMs (SP7472100-XXX). The local SRAM has a memory capacity of 1 Mbyte. The memory module used allows zero wait-state access at the 16-MHz processor clock frequency. The memory is organized 32 bits wide and supports all access modes of the 68030.

4-12.3 Serial I/O Interfaces

The MCP contains two RS-232 serial I/O interfaces built around the multiprotocol communications controller (MPCC). The serial interfaces are connected to two 9-pin D-sub connectors on the front panel. One of the two serial interfaces can be reconfigured for RS-422/RS-485 compatibility. Each MPCC interfaces a single serial communication channel using synchronous or asynchronous protocol. In addition to data transfer between the CPU and MPCC, control and status are provided through the 22 directly addressable registers. The on-chip oscillator drives the internal baud rate generator which with two selectable prescalers and a 16-bit divider provides baud rates from 110 to 38400 baud.

4-12.4 MPCC Interrupt Handling

Two bus interrupter modules (BIMs) are used to handle all local interrupts. Each MPCC is able to force an interrupt on three different conditions: receiver contains a character, the hardware interface has detected an interrupt generation state, or transmitter is empty. The three different groups of interrupt generation are under software control through some of the 22 registers of the MPCC. The BIM provides a flexible interrupt structure because the interrupt level and the interrupt vector are software-programmable. This allows the adaptation of the RS-232 interface on the main board to a wide variety of applications. The two parallel interface and timer (PI/T) devices are used for local control. One port is assigned for interrupt level control and one other port is used for reading the rotary switches on the MCP. The rotary switches can be used as a general-purpose input channel for diagnostics, configuration selection, or automatic system boot with different configurations.

4-12.5 VMEbus Interface

MCP VMEbus supports 8-, 16-, 32-bit, and unaligned data transfers. The extended, standard, and short I/O address modifier codes are implemented to interface to all existing VMEbus products. Each of the seven interrupt request signals can be connected to the implemented interrupt handler. A single-level bus arbiter and the bus arbitration, which has four bus release options, completes the VMEbus interface.

4-12.6 MCP Function Switches and LEDs

The MCP contains four function switches and seven LEDs for board function control. The switches and LED functions are as follows:

a. A reset of all onboard I/O devices and the FPCP is enabled if the RESET switch is pushed to the “up” position. RESET is held active until the switch is in the “down” position.

In addition, a local timer guarantees a minimum reset time of two to three seconds. Power fail and power up also force a reset (2-3 seconds) to start the board if the supply voltage is out of range (below 4.75 volts).

b. The ABORT switch, which provides an interrupt on a software-programmable level, is provided on the board to allow an abort of the current program, to trigger a self-test, or to start a maintenance program. ABORT is activated in the “up” position and deactivated in the “down” position.

c. The CACHE switch enables the 68030 onchip data cache with its 256 bytes when in the “down” position. In the “up” position, the onchip cache is deactivated by hardware, overriding all software settings. IR uses this switch in the “down” position for normal operations.

d. The RUN/HALT (R/H) switch enables or disables local operation of the CPU and the FPCP. This switch can be used to debug multiprocessor software packages and to disable a CPU board in an application when a failure has occurred but power can’t be switched off. The processor is in the halt state if the switch is in the “up” position. Normal IR operation is provided when the switch is in the “down” position.

e. The RUN LED is green if the processor is not in the halt state. It is red during the reset phase, and when the processor is in the halt state.

f. The SRAM LED is always lit yellow when the processor is accessing the local SRAM.

g. The EPROM LED is lit yellow when the processor accesses the EPROM area.

h. The bus request (BR) VME LED is lit yellow when the local processor requests bus mastership on the VMEbus.

i. The bus master (BM) LED is lit when the MCP is the current bus master.

j. The data strobe (DS) VME LED is lit whenever the processor has placed a data strobe on the VMEbus.

k. The DS VSB LED is lit whenever the processor has placed a data strobe on the VSB. Not applicable to IR operations.

l. The rotary switches are 4-bit hexadecimal encoded. They are completely under software control. Normal IR operation is with the switches in the “F” position.

4-12.7 BERR Handling

The MCP contains a timeout counter to detect if an addressed device or memory does not respond with a DSACK to the CPU. The timeout is fixed, set to 70-80 microseconds, allowing slow VMEbus boards to communicate with the CPU.

4-13 Acquisition Processor

Refer to figure 4-10 for the following ACQR functional description. The address select enables the control logic section of the ACQR by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining eighteen address lines (A18-A01) are then used by the control logic to determine the function to be processed.

4-13.1 VMEbus Interrupts

The ACQR asserts IRQ4* following completion of the TD interval. During the interrupt acknowledge cycle, ACQR outputs a vector as programmed in the vector mask register. The following is a memory map of the ACQR:

Offset from ACQR	Base Address Function
$000 - $001	Write: Control and Vector Mask Register Read: Peak Bin Index Register
$800 - $FFF	Read: Bin Storage RAM

4-13.2 Acquisition Data Processing

The ACQR receives 8-bit correlator sums from either one or both DMSSs. (These data are in two’s complement form). Each DMSS provides two sums: one for the I component of that channel, and one for the Q component. The number of

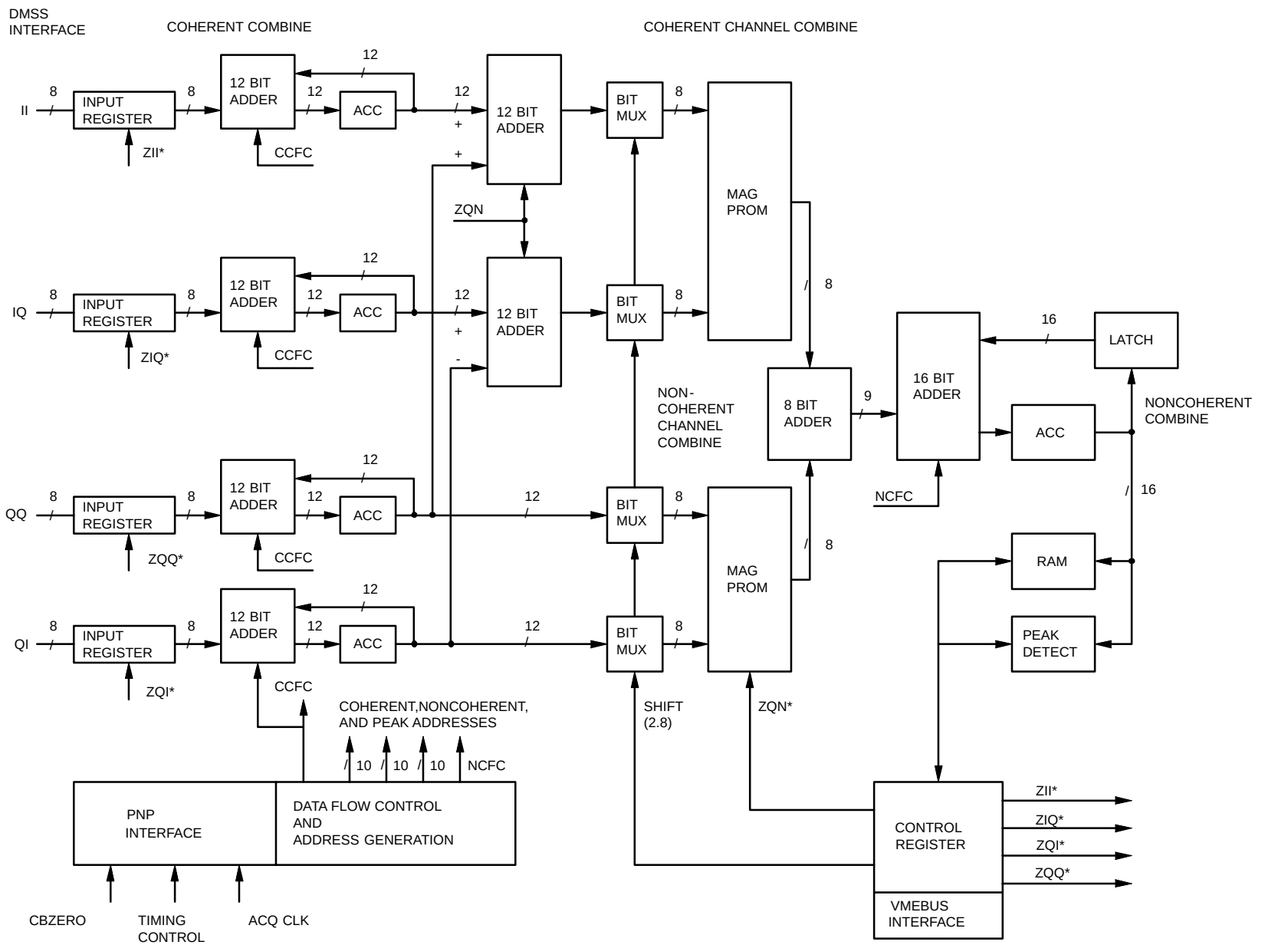


Figure 4—10. ACQR Functional Block Diagram

coherent and noncoherent combines is determined by the timing signals coming from the PNP. The data is clocked into the ACQR with the rising edge of ACQCLK, at a rate not to exceed 6.5 MHz. See figure 4-11 for examples of the combining process within the ACQR.

4-13.3 Coherent Combine

Each sum is accumulated from 0 to N times, providing a coherent combination with twelve bits of resolution. N is determined by the period of TCOHB; for N greater than fifteen, overflow is possible for certain input signals. Accumulating zero times means that the output of this stage at time T is equal to the input at T-1. Accumulating one time means that the output is equal to the sum of the inputs at time T-L-1 and time T-1, where times T-1 and T-L-1 are in the same interval. (L is the correlator length on the DMSS.) The output of this stage is a sequence of L sums, with each sum corresponding to a correlator bin location.

4-13.4 Coherent Channel Combine

The coherent combine sums from each channel may be combined with the corresponding sum from the other DMSS, (i.e., the I_I (I DMSS, I component) coherent combine sum is added to the Q_I (Q DMSS, I component) coherent combine sum, and the I_Q and Q_Q sums are similarly combined). This function is enabled or bypassed depending on the contents of the control register.

4-13.5 Magnitude PROMs

Only eight bits from the coherent or coherent channel combines are input to the magnitude PROMs; selection of which eight is determined by the contents of the control register. The magnitude of the signal output from the coherent (channel) combines is determined for each channel by the PROMs.

4-13.6 Noncoherent Channel Combine

The magnitudes of the two channels are added in this stage if the control bit in the control register is set; other wise, the Q channel input to the adder is zeroed.

4-13.7 Noncoherent Combine

The outputs from the noncoherent channel combine are accumulated from 0 to N times, as determined by the PNP timing control signals. Since the input from the noncoherent channel combine may be nine bits, overflow may occur for N greater than one-hundred twenty-seven for some input signals. (The accumulated sum is sixteen bits.) To minimize errors in peak detection and data processing due to overflow, output values from this stage is limited at $FFFF.

4-13.8 Peak Detection

Following the last noncoherent combine accumulation for an interval or subinterval, a peak search is performed in hardware. The location of the bin containing the peak value is stored in the peak bin index register.

4-14 PN Processor

Refer to figure 4-12 for the following PNP functional description. The address select enables the control logic section of the PNP by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining eighteen address lines (A18-A01) are then used by the control logic to determine the function to be processed.

4-14.1 PN Code Generation

4-14.1.1 The PNP generates two dual PN code strings. One of the code strings is called the tracking PN code and the other is called the acquisition PN code, each having an I component and a Q component. The I part of the code is 1/2 chip ahead of the Q part. Each string has its own NCO to control its frequency. The NCOs have a frequency range of 4 MHz to 13 MHz and can be set to run at the PN code rate, twice the code rate, or at four times the code rate.

4-14.1.2 If the PN code rate is less than 4 MHz, the codes are generated from RAM look-up

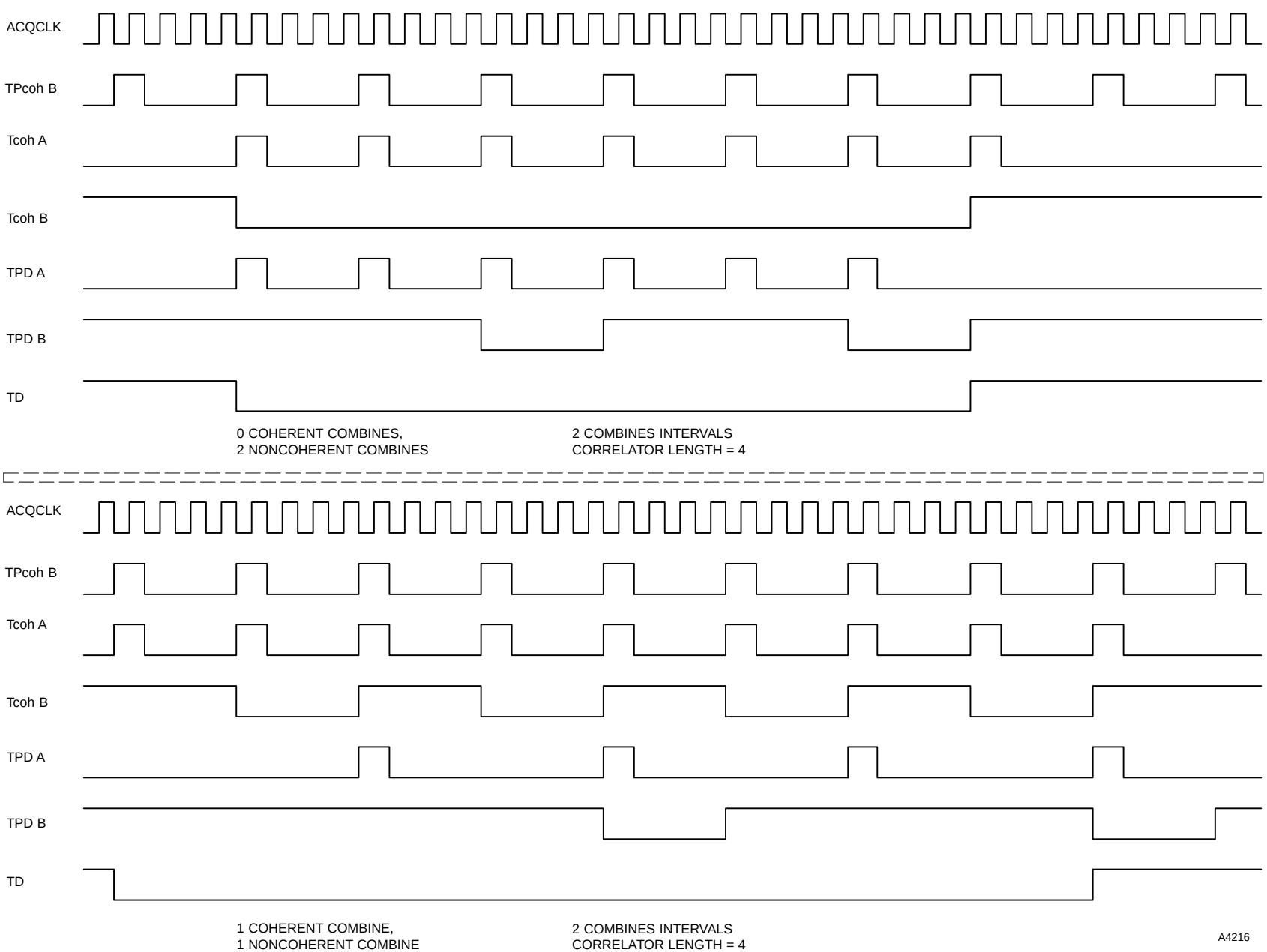


Figure 4—11. ACQR Timing Diagram

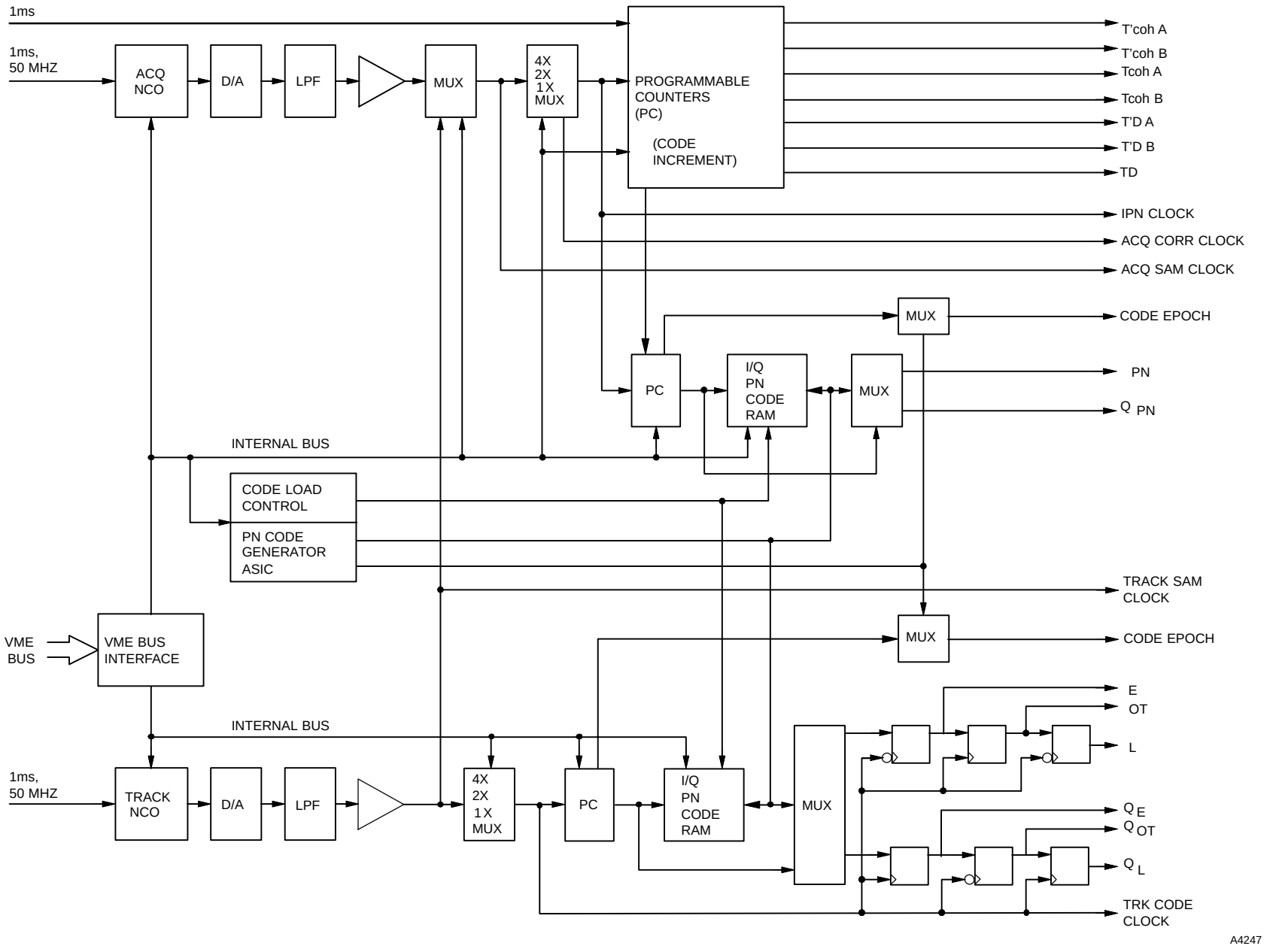


Figure 4—12. PNP Functional Block Diagram

tables. The PN code RAM can be loaded from the VMEbus or auto-loaded with the PN code generator chip and is adjustable from 1 to 262,144 bits in length. Both NCOs and PN code generators are updated at the 1-msec timing mark after their registers are set. Each NCO (and code generator) have an independent reset. Once the code generators are running, the code offsets are relative to the current code state. The code generators are initialized to the zero state.

Note

The maximum length registers must be set in both of the code generators before starting the auto—load function.

4-14.1.3 The tracking PN code generator generates the early, late, and ontime codes for both I and Q components. The early and late signals are half a chip off of the ontime and have a maximum skew of 6 nanoseconds. The acquisition PN generator outputs are inphase (within 15 nanoseconds) with the ontime outputs of the tracking PN generator, as long as both NCOs and code generators are given the same control information. If the PN code rate is higher than 4 MHz (high-rate PN), the PN code generator chip generates the output PN code directly. Only the I PN code is used in this mode. The acquisition sample clock controls the code rate in this mode.

4-14.2 PN Code Generator Chip

The PN code generator chip is comprised of three coders (32-bit shift-registers with programmable feedback). In the high-rate PN mode, only one of the shift-registers (coder 0) is used to generate the PN code. In the auto-load mode, coder 0 is used for the I code and coder 2 is used for the Q code. The output of coder 1 may be XORed with the output of either (or both) coder 0 and coder 2 before the PN code is stored in RAM.

4-14.3 Programmable Counters

4-14.3.1 The acquisition PN clock also drives four cascaded programmable counters. The four programmable counters provide timing signals for the acquisition process. See figure 4-11 for an example of the timing signals sent to the ACQR. The first counter, T'COH (TP_{coh} B), has ten bits and is set to count the length of correlators. The value set in this register is the correlator length (4-1024) minus one. The second counter, TCOH (T_{coh} A/B), has five bits. The value set in this register is number of coherent combines (0-31). The third counter, T'D (TPD A/B), has eleven bits. The value set in this register is the number of noncoherent combines (0-2047). The fourth counter, TD, has seven bits. The values set in this register is the number of subintervals (1-127). When the value in this register is greater than one, the acquisition code generator is incremented by the value stored in the ACQR code increment factor register (from 0 to 1023) for each additional subinterval.

4-14.3.2 The output of bit 15 of the PNP control register drives a pin on the P2 connector and is called PN LOCK. Bit 10 of the control register controls whether the acquisition sample clock is the output of the acquisition NCO or the output of the tracking NCO (making the acquisition sample clock the same as the tracking sample clock).

4-15 Timing Generator

Refer to figure 4-13 for the following TIME functional description. The address select enables the control logic section of TIME by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining 18 address lines (A18-A01) are then used by the control logic to determine the transfer function to be processed.

4-15.1 IRIG Decoding

TIME provides the capability of decoding unmodulated IRIG-B data into components of seconds, minutes, hours, and days, and to buffer these signals to the data lines on the VMEbus when enabled by the control logic. The IRIG-B data is updated and written to RAM between the 0 msec and 500 msec marks. The data is valid for reading from RAM between the 500 msec and 0 msec marks. The time components are in binary-coded decimal (BCD) format.

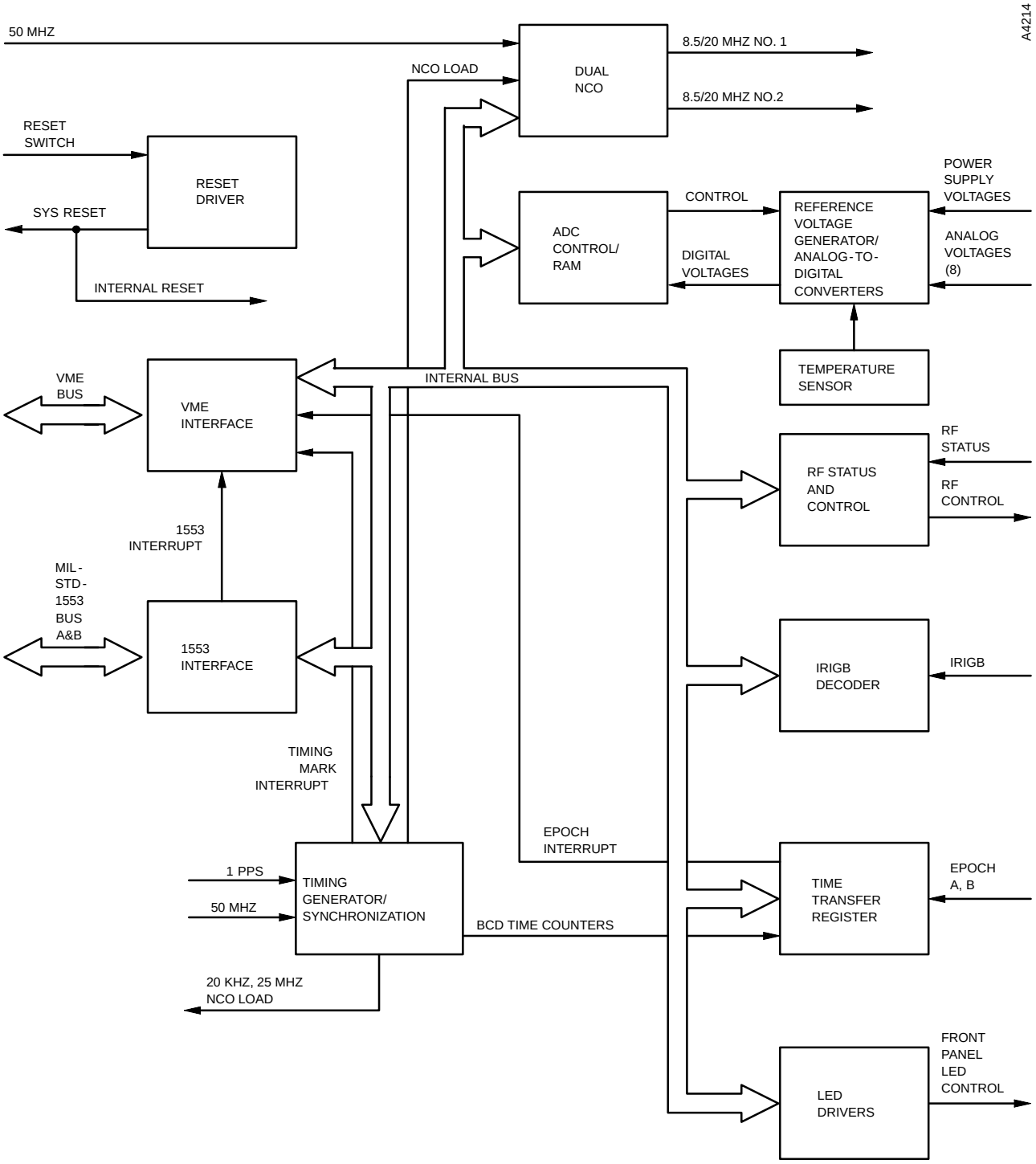


Figure 4—13. TIME Functional Block Diagram

4-15.2 1553 Bus Interface

TIME provides a transformer-coupled 1553 interface between the VMEbus and the P2 connector. The interface to the P2 connector consist of two transmit/receive transformers and the remote terminal address inputs. The interface to the P1 connector consists of the address and data lines to read/write to 1553 control/status registers and RAM.

4-15.3 Time Mark Generation

TIME generates 1-, 10-, 100-, 1000-, and 20,000-PPS time marks based on the 50-MHz input in sync with the 1-PPS external signal. The time marks have a duty cycle of 20% and are valid on the falling edge of the pulse. A status indicating the detection of a time synchronization error between the external input 1-PPS and the internally generated 1-PPS is provided in the TIME status word. The time synchronization error is set if the 1-PPS external and 1-PPS internal signals differ by more than one 50-MHz clock cycle. A time resynchronization may be commanded through the TIME control register. There is also a flag that is set when the resynchronization process is complete.

4-15.4 Interrupt Generation

TIME provides interrupt to the VMEbus consisting of the generated time marks, the 1553 bus interrupt, and the selected epoch interrupt. Any or all of the interrupts can be masked through the interrupt mask register. The interrupts are divided into two separate groups: time interrupts and other interrupts. Each group has a programmable vector in which the upper nibble is determined by the interrupt vector register. The lower nibble is determined by the interrupt generated. The time interrupts interrupt the microprocessor with a level 6 interrupt and the other interrupts with a level 3 interrupt.

4-15.5 Epoch Count Generation

TIME provides the time difference between the epoch A or B and the 1-PPS signal with 100-nanosecond resolution when enabled by control logic. This time difference is valid upon the epoch interrupt of the microprocessor. The difference components are in BCD format. The epoch is selectable between A and B through the TIME control word.

4-15.6 NCO Outputs

TIME provides two NCOs that are controlled by the MCP program (via the VMEbus). The NCOs have a sampling frequency of 50 MHz and a 22-MHz lowpass filtered analog output of these NCOs is available through coaxial connectors J1 and J2.

4-15.7 Analog-to-Digital Generation

4-15.7.1 TIME provides a digital measurement of various analog voltages to the data lines on the VMEbus when enabled by control logic. There are 16 possible measurements, and the measurements are updated and written to RAM between the 800 msec and 0 msec marks; therefore, the measurements are valid for reading from RAM between the 0-msec to 800-msec marks. Channels 0-7 are predefined and channels 8-15 are user defined. The analog level value register output value is dependent upon the channel being read. The output range is +/-10 volts, and the LSB is equal to 4.88 millivolts. The output is in offset binary format meaning 0000H = -10 volts, 0800H = 0 volts, and 0FFF = +10 volts.

4-15.7.2 The channels are defined as follows: channel 0 is the -5.2 Vdc and +5 Vdc supply sum, channel 1 is the -12 Vdc and +12 Vdc supply sum, channel 2 is the -15 Vdc and +15 Vdc supply sum, channel 3 is ground, channel 4 is the -6.2 Vdc reference, channel 5 is the +6.2 Vdc reference, channel 6 is the temperature sensor, and channel 7 is the RF 5 Vdc supply. The temperature sensor voltage to degrees C conversion is as follows: 15.0 C = +5.764 volts, 20.0 C = +5.864 volts, 25.0 C = +5.964 volts, 30.0 C = +6.064 volts, etc.

4-15.8 Miscellaneous Registers and Control

The TIME test point register provides up to eight test points on the TIME via the P2 connector controllable from the VMEbus. Each point is cleared or set through the corresponding bit in the

test point register. The TIME driver register provides eight bits of control adjustable by control from the VMEbus. This register interfaces to the P2 connector to drive various signals. The TIME also provides the capability of reading a reset switch from the P2 connector and drive SYSRESET* on the P1 connector to reset the unit when this switch is closed for a minimum of 200 msec.

4-15.9 RF Status and Control

The RF modules provide TTL level RF status signals which provide up to 8 bits of RF status information to the VMEbus upon command. Subsequently, 8 bits of adjustable control are generated for use by the RF modules.

4-16 Demodulator Processor

Refer to figure 4-14 for the following DMDP functional description. The VMEbus address select enables the control logic section of DMDP by matching address lines A23-A19 of the VMEbus address with the board select bits of the P2 connector. The remaining eighteen address lines (A18-A01) are then used by the control logic to determine the function to be processed. DMDP asserts IRQ5* following either of the VMEINT registers being accessed by TMS bus.

4-16.1 TMS Bus Interface

The DMDP is controlled by a digital signal processor (DSP), the TMS320C25 (TMS). Code executed by the TMS controls and receives data from the OUTP and DMSSs; generates interrupts to the VMEbus; sends status to the MCP over the VMEbus; receives control and configuration data from the MCP; directs the FFT controller (FFTC), a TMC2310; and loads up to eight 8-bit DACs.

4-16.2 Local TMS Bus

Within the local TMS bus address space, the following functions are found:

a. On-Chip Memory. This memory is zero wait-state and there are 544 words available.

b. Off-Board Memory Space. This memory-mapped space is set up for two wait-state (<240 nanoseconds at 40 MHz) access.

c. VME Dual Port RAM (Side A). The interface with the VMEbus for passing status and control is set up for one wait-state (<140 nanoseconds at 40 MHz) access. This DPRAM is of the 2k x 16 bits size.

d. DAC Registers. Eight D/A converters are under TMS control. They appear as unique 8-bit write-only memory locations with 2 wait-state access. They are used to provide AGC and dc-bias compensation to the RF portion of the tracking loops. Output from each DAC is +10.0 x (VALUE/256) volts, where VALUE is the unsigned 8-bit number written to the DAC. The address offset for each DAC is the DAC number (0 through 7). (The VMEbus address offset is 2 x (DAC#).)

e. FFT DPRAM. The FFT DPRAM is size 2k complex words (2k x 2 x 16 bits). This memory also is accessible to the TMS bus as 1 wait-state memory when the TMS control register is configured to permit access. The memory is partitioned into 2k words each for the real and imaginary components.

f. Local Data Memory. This memory is zero wait-state access; minimum size is 4k words, with expansion capability to 32k words.

g. Program ROM. Executable code (SP7472110-xxx (J11 and J12), where xxx represents the release version) is stored in 2 wait-state ROM. Initialization code copies from ROM to program RAM prior to setting the RAM selection bit in the TMS control register. (This space is shared with program RAM.)

h. Program RAM. This memory is zero wait-state. When ROM is selected by the TMS control register, the actual data RAM is not accessible; program RAM occupies the same space. When RAM is selected by the control register, this RAM occupies the same space as ROM did; data RAM is then accessible.

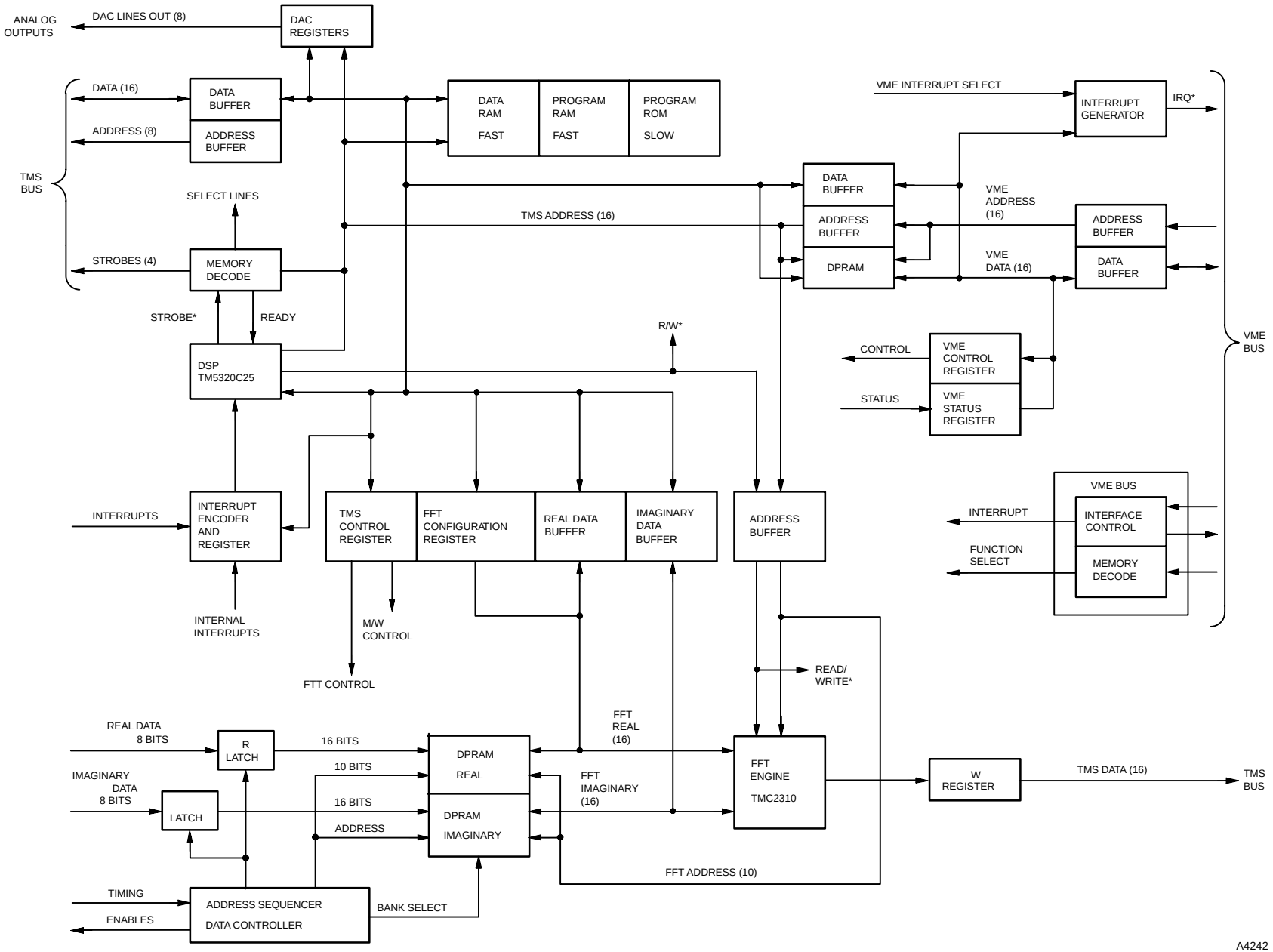


Figure 4–14. DMDP Functional Block Diagram

4-16.3 External TMS Bus

A portion of the TMS memory space is reserved for off-board access. This space is divided into four quadrants of 256 words each; accessing a quadrant enables the corresponding STROBE signal (1-4) for controlling data transfer. This memory space is required to have memory access time of less than 240 nanoseconds (2 wait states at 40 MHz). See figure 4-15 for timing specifications.

4-16.4 FFT Controller Operation

The FFTC performs FFT and magnitude squared operations when directed by the TMS control register. In order to properly control the FFTC, the following sequence of operations must be performed for each function required:

a. Reset the FFTC by setting the command bit to 00b.

b. Write the first required configuration code to FFTC configuration data register (FFTCNF).

c. Load the FFTC configuration register by setting the command bits to 01b.

d. Set the command bits to 11b to deactivate the command bits.

e. Write the second required configuration code to FFTCNF.

f. Repeat steps c and d.

g. Send a start command to the FFTC by setting the command bits to 10b.

h. Repeat step d.

i. When done, the FFTC asserts a signal to generate an interrupt to the TMS.

4-16.5 FFT Data Collection

The input data to the FFT DPRAM is selected from DMSS (I) or DMSS (Q) by the TMS control register. Since both sources may be selected and there is one set of input lines, the data input process is time-division multiplexed to be written into the respective memory bank in the DPRAM; DMSS (I) data to bank 1, DMSS (Q) data to bank 2. The FFT is performed in place; therefore, the data is stored in locations corresponding to the bit-reversal of the address. Data collection at rates up to 50 kHz is supported.

4-16.6 Zero Filling of FFT Data

Zero filling is accomplished by forcing input data sample N+1 through 2N to be identically equal to zero; i.e., samples 1 through N are input from the selected DMSS, while the memory locations corresponding to samples N+1 through 2N are loaded with zero. This function is selected by the TMS control register.

4-16.7 VMEbus Interface

The DMDP interfaces with the VMEbus as a slave and as an interrupt generator. It uses standard addressing with a 16-bit data bus (A24:D16). Base address is selectable in 512k blocks by connecting the appropriate selection lines to ground in the unit (unused base address selection lines are pulled up to +5.0 Vdc).

4-16.8 VMEbus Interrupts

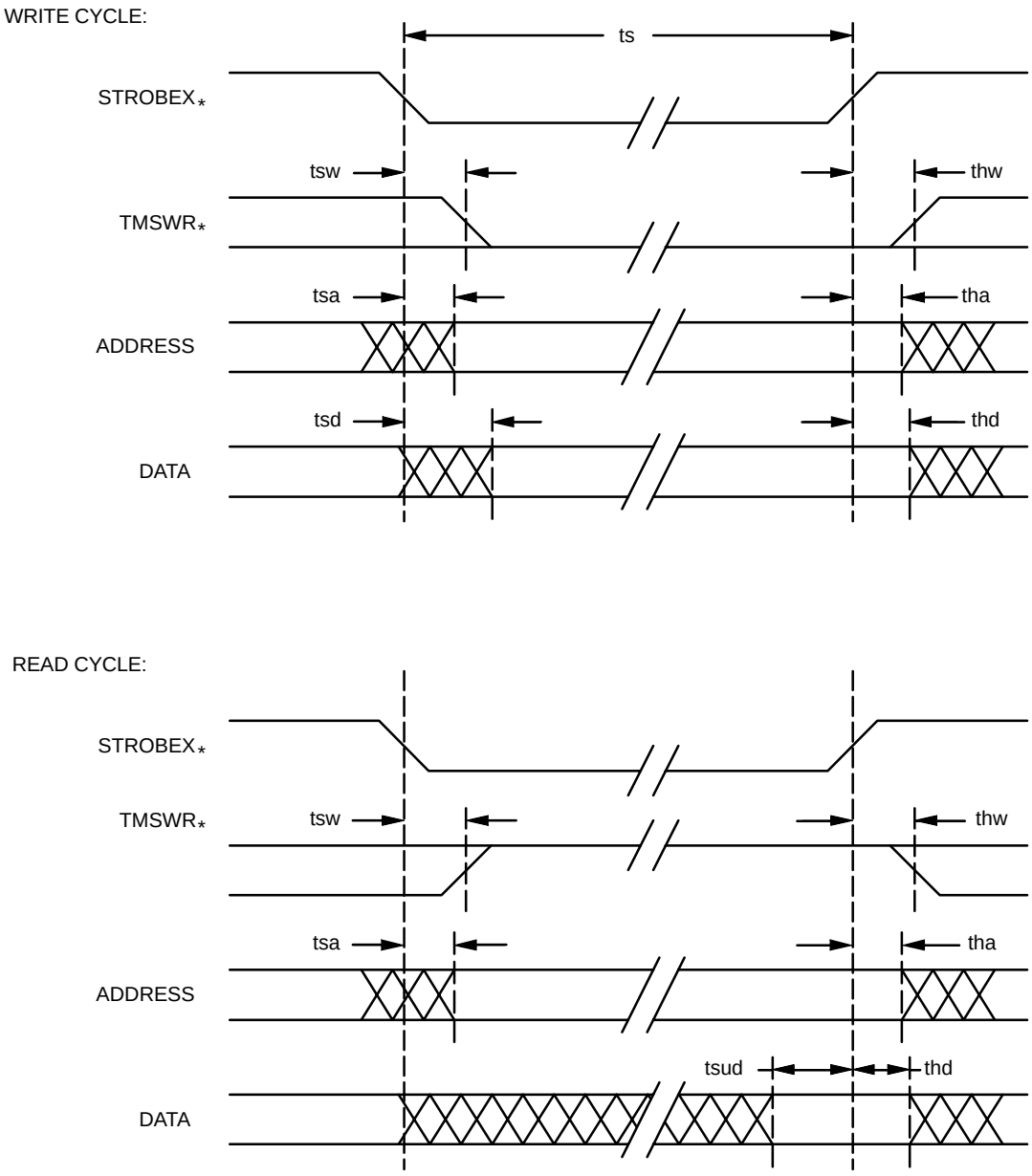
The DMDP asserts IRQ5* following TMS access of either VMEINT register. During the interrupt acknowledge cycle, the DMDP outputs a vector to correspond with which register was accessed. Bit 1 of the vector corresponds to VMEINT1 being accessed and bit 0 of the vector corresponds to VMEINT0 being accessed. Bits 7-2 are programmable from the VMEbus by writing to the vector mask register.

4-16.9 VMEbus Registers

Accesses to the I/O register spaces are zero wait-state for write and one-wait state for read. Functional descriptions are listed below.

a. Hardware Control Register and Vector Mask Register. These registers are accessible one byte at a time, or as one word. (Bits 15-8 go to a logic 0 following hardware reset; states of bits 7-2 are indeterminate following power-up).

A5338



TIMING SPECIFICATIONS

tsw	≤	32 ns
tsa	≤	9 ns
tsd	≤	40 ns
tsud	≥	51 ns
tha	≥	0 ns
thd	≥	0 ns
thw	≥	0 ns
ts	~	200 ns

Figure 4—15. TMS Bus Timing Diagram

b. TMS Interrupt Generation Register (INTGEN). When this write-only register is accessed, an interrupt is generated to the TMS. This is used to indicate that new control information is present in the VME DPRAM.

c. Status Register (STAT). This read-only register is available to read hardware status from DMDP.

4-16.10 VME Dual Port RAM (Side B)

The interface with the TMS bus for passing control status information. This DPRAM is of the 2k x 16 bits size.

4-16.11 Test Mode

The DMDP operates in test mode when so directed by the VME control register. In test mode, TMS operation is inhibited. The VMEbus can then logically extend onto the TMS bus for memory, functional, and closed-loop test. All accesses to the TMS bus are mapped into an appropriate space on the VMEbus.

4-17 Output Processor

Refer to figure 4-16 for the following OUTP functional description. The address strobe signal (STROBE3*) enables the control logic section of the OUTP to accept the valid address input on lines TADD7-TADD0 of the TMS bus. The eight bits are then used by the control logic to determine the function to be processed.

4-17.1 SSA Combining

The OUTP provides the capability of accepting 5-bit sign-magnitude I and Q symbol streams and combining them with baseband demodulated sign-magnitude I and Q signals from a second co-located IR. The maximum rate of these data streams is 6 Mbps. Combiner synchronization is achieved by various methods. In one method, the user programs the combiner maximum count and threshold registers. The maximum count is an 8-bit value determining the number of symbols counted in the combiner lock test. The threshold is an 8-bit value such that when the number of symbol sign matches exceed the threshold, combiner lock is achieved. The combiner automatically goes through the possible combinations of the combiner input data crossover and/or negation and the symbol data delays until the data is aligned properly. Any or all of the combiner lock combinations can be manually set by setting the bypass sync control bit and the desired combination. LEDs on the OUTP front panel provide the lock status of the I (DS4) and Q (DS5) combiners.

4-17.2 I and Q Deinterleaving

The OUTP provides the capability of I and Q deinterleaving and decovering when enabled by the control logic. The deinterleaver is a (30,116) periodic convolutional deinterleaver and the decoverer consists of a 30-bit sequence used to invert/not invert the deinterleaver output data. The I and/or Q deinterleavers are enabled by setting the bits in the decoder/deinterleaver control register.

4-17.3 I and Q Decoding

4-17.3.1 The OUTP provides the capability of decoding dual decoded I and Q symbols when enabled by control logic. The dual decoding function handles rate 1/2 and rate 1/3 decoding and accepts three bit soft-decisioned in-sign magnitude. The dual decoder is a Viterbi decoder with polynomial coefficients of constraint length 7 as follows:

G1 = 1111001
G2 = 1011011
G3 = 1110101

4-17.3.2 In all modes, the decoder/deinterleaver control register and the dual decoder write registers must be set for proper synchronization and operation of the I and Q decoding function. LEDs on the OUTP front panel provide lock status of both the I (DS1) and Q (DS2) decoders. The dual decoder is capable of the following modes:

a. Rate 1/2 serial: This mode allows the I or Q data to be fed directly into the decoder R0 port resulting in rate 1/2 decoding.

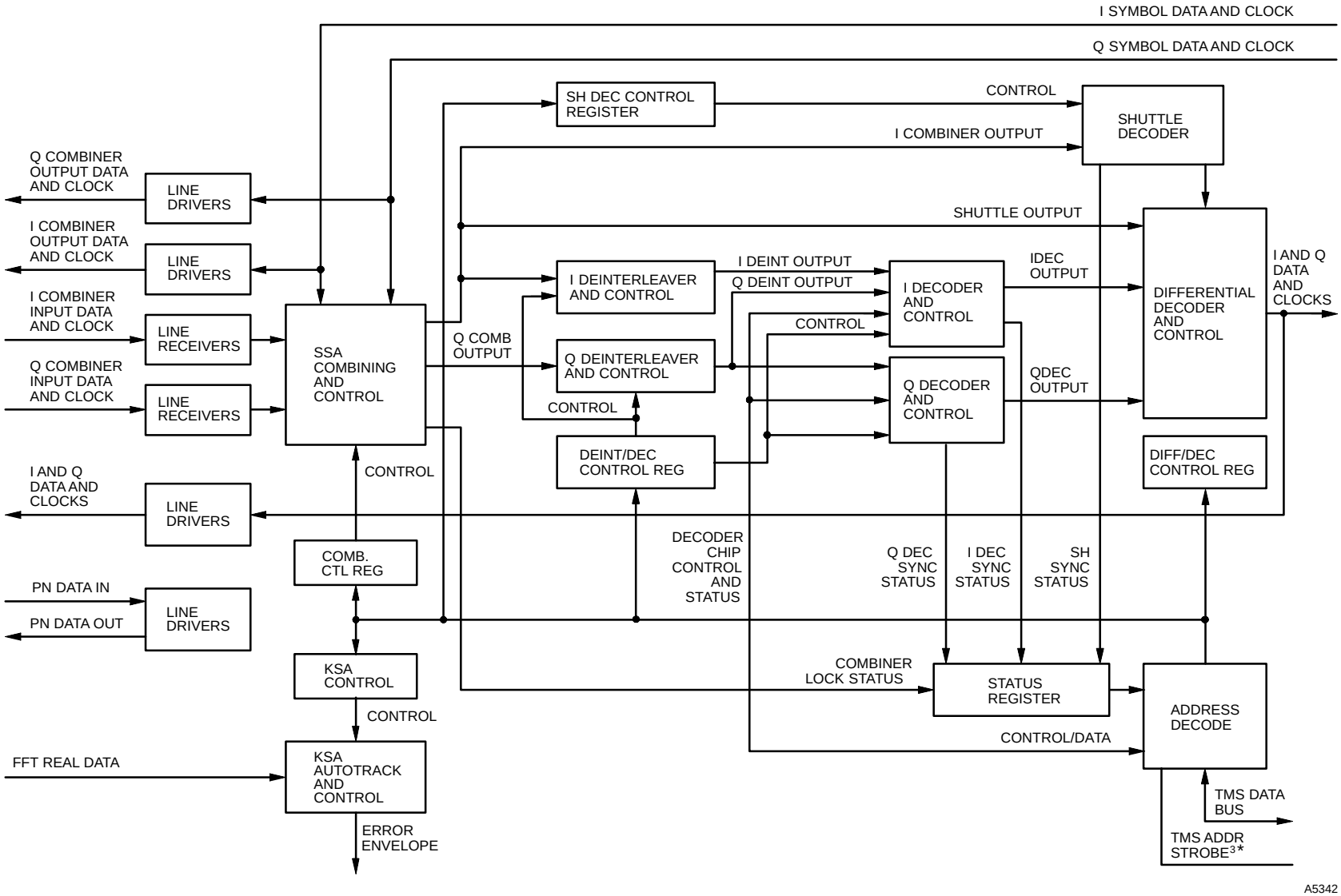


Figure 4—16. OUTP Functional Block Diagram

b. Rate 1/2 parallel: This mode allows swapping of I data R0 and R1 input ports. It also provides the capability of piping in the Q data into the I decoder R1 port.

c. Rate 1/3 serial: This mode allows the I or Q data to be fed directly into the decoder R0 port resulting in rate 1/3 decoding.

4-17.4 Shuttle Decoding

4-17.4.1 The OUTP provides the capability of outputting Shuttle decoded I symbols when enabled by control logic. The Shuttle decoder has a rate 1/3, three-bit soft-decisioned in-sign magnitude, parallel loaded, Viterbi decoder with polynomial coefficients of constraint length 7 as follows:

G1 = 1111001
G2 = 1011011
G3 = 1100101

4-17.4.2 The Shuttle decoder control register must be set for proper operation of the Shuttle decoding function. The disabling of the reset bit allows the Shuttle decoder function to begin synchronization. The Shuttle decoder automatically tries to synchronize itself unless the SYNCCTL bit is set. If SYNCCTL is set, the other bits in the control register are used in the manual mode in an attempt to sync. An LED on the OUTP front panel provides Shuttle decoder lock status (DS3).

4-17.5 KSA Autotrack

The OUTP provides the capability of generating a KSA autotrack error envelope signal from the I or Q demodulator (whichever has the highest signal-to-noise ratio as selected by TMS). The KSA autotrack constants are related to the I or Q demodulated output. The KSA autotrack signal output is a D/A converted, filtered signal with a maximum differential voltage of 12 V p-p.

4-17.6 Differential Decoding

The OUTP provides the capability of differentially decoding the I and Q output bits when enabled by the control logic. Differential decoding consists of converting the output bits from NRZ-S or NRZ-M to the NRZ-L format. Setting of the proper bits in the differential decoder control register enables this function.

4-17.7 I and Q User Data Outputs

The OUTP provides the capability of selectable outputs for the I and Q user data. Selection of the I and Q outputs are contained in the differential decoder register. Possible selections for the I output include: I combiner output sign bit, Shuttle decoder output, I dual decoder output, and toggled I and Q output (in that the I and Q data is toggled out at the rising and falling edges of the data clock). Possible selections for the Q output include: Q combiner output sign bit and Q dual decoder output.

4-17.8 OUTP Status Registers

The OUTP provides status of the board in the form of the following two registers:

a. Status register 1 contains information on the lock status of the combiner, the Shuttle decoder, and the dual decoder for both I and Q channels. Status register 1 also contains information on whether the particular lock status has changed since the last reading of the register (i.e., if the I decoder shows locked, whether the I decoder has dropped lock since the last read).

b. Status register 2 contains information on the current sync state of the Shuttle decoder and the modulo count of the number of times the I and Q decoders have changed sync state.

4-18 Demodulator Symbol Synchronizer

Refer to figure 4-17 for the following DMSS functional description. The address strobe signal (STROBE*) enables the control logic section of the DMSSs to accept the valid address input on lines TADD7-TADD0 of the TMS bus. STROBE1* enables DMSS (I) and STROBE2* enables DMSS (Q). The 256 locations assigned to the DMSSs are decoded as follows:

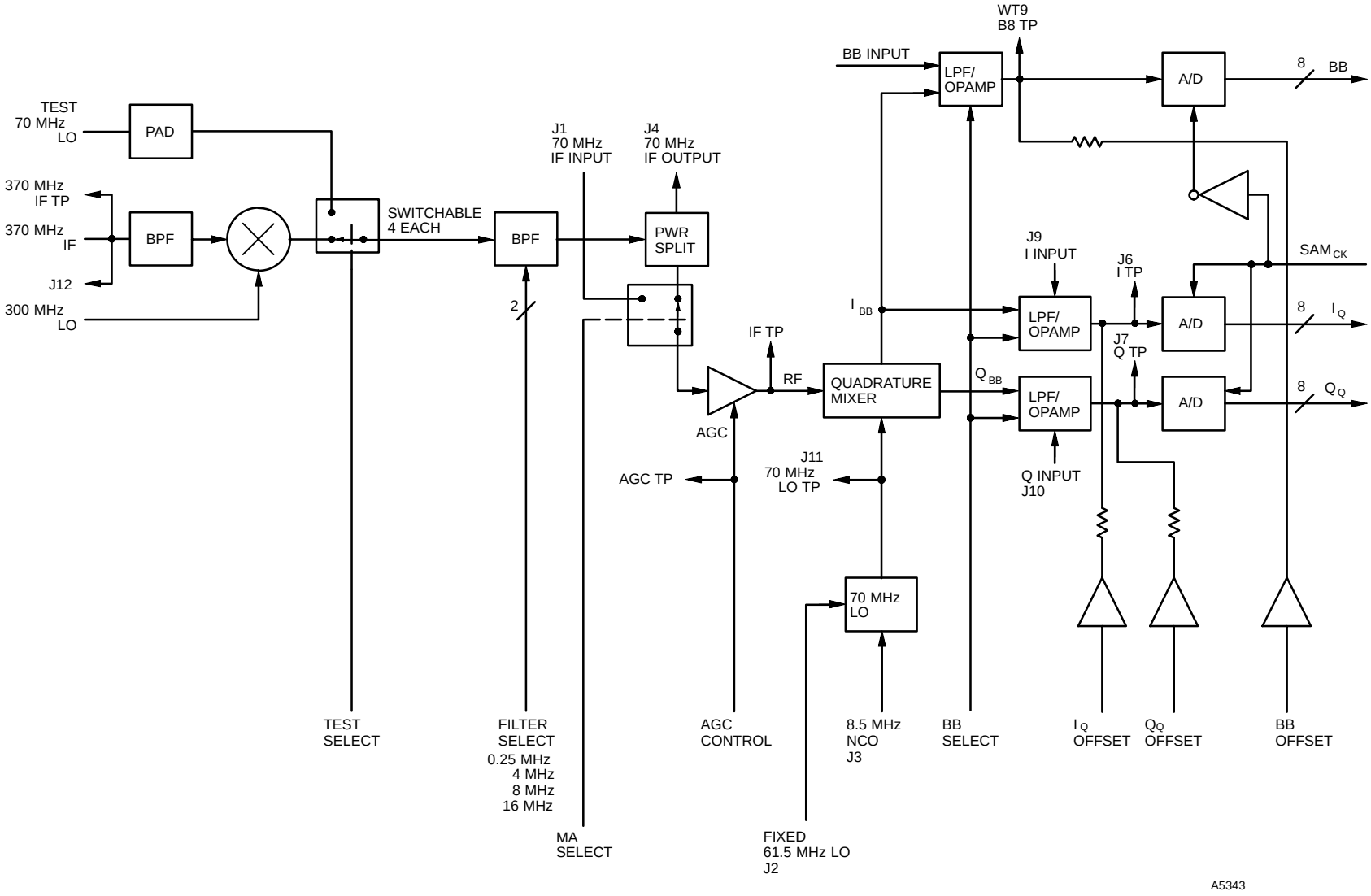


Figure 4–17. DMSS Functional Block Diagram

Address	Function
00 - 3F	Demod chip
40 - 4F	I channel acquisition correlator
50 - 5F	Q channel acquisition correlator
60 - 7F	Reserved
80	Control register 1 (write and read)
81	Control register 2 (write and read)
A0 - FF	Reserved

4-18.1 FIR Filters

The 8-bit digitized I and Q components of the return service signal are input to two independent finite impulse response (FIR) digital filter chips. The filters contain eight cells with nine bits of data and coefficients. The output of the filters are used for further DMSS processing or output to the other DMSS. The filters perform the following functions:

a. The filters are able to perform decimation by the values of 1, 2, or 4. The coefficient for all decimation and bypass modes are stored in the PROM and selection is based on the mode and done by the DMDP. There are sixteen sets of coefficients for each mode. There is one set of coefficients for bypass mode. The coefficients for bypass mode are stored in decimation by one section of the PROM and are all “0”s and one “1”.

b. The filters are operated in sample rates ranging from 500 ksps to the maximum of 25 msps.

c. Output from the filters is up to twenty-five bits. Only eight bits from the filters are input to the Demod chip. Selection of which eight bits is determined by the value of the three control bits in control register 2.

4-18.2 Demod ASIC

The FIR filtered I and Q and the input baseband/subcarrier signals are processed in parallel using the Demod chip. The input to the Demod chip is either the output of the FIR filters or the input from the other DMSS. The Demod chip performs the following functions:

a. Provides integrate-and-dump filtering, timing error detection, phase-error detection, symbol timing acquisition and tracking, timing loop filtering, and data AGC control functions for the I and Q data paths.

b. Provides PN despreading and tracking functions in the spread mode. The Demod chip also provides for the early/late PN timing error detection, noise estimation, and I/Q power level measurement.

c. There is an NCO in the Demod chip that is clocked at 70-MHz. The maximum output frequency of this NCO is 25 MHz.

d. Provides for single channel combine where the output of the single channel from one Demod chip is input to the other Demod chip of the other DMSS. This combining process increases the signal-to-noise ratio by 3 dB.

e. The Demod chips in both DMSSs are synchronized together by a TMS service routine that enables both chips for synchronization on the rising edge of the 20-kHz clock.

4-18.3 Squaring PROMs

The six bits of I and Q data symbols, processed by the Demod chip, are passed on to a squaring PROM that performs complex squaring or quadrupling functions. There are eight sections in the PROM. One of the sections is used for squaring and the other seven sections for quadrupling functions. The DMDP selects the desired section. The real and imaginary PROM results are input to the Demod chip and after further processing, are output from the DMSS as the complex FFT data to the DMDP.

4-18.4 Scaling PROMs

The six bits of 2’s complement I data symbols are input to a scaling PROM to perform scaling and format conversion functions. The PROM output is scaled based on the scaling factor from the TMS and converted to five bit offset binary. These five bits and the associated symbol clock are output from the DMSS in TTL logic to the OUTP. The MSB of the I symbol and symbol clock are also converted to ECL and output.

4-18.5 Acquisition Correlators

4-18.5.1 DMSS contains two, multi-tap, flexible correlators, variable in length from 4-to-1024 taps to provide PN code acquisition. The correlators generate correlation values for two serial bit streams (bit 1 and bit 0). The new PN code is loaded into the correlators on the rising edge of the Tcoh clock. The inputs to the correlators are either from the FIR filters on the DMSS or from the other DMSS. The acquisition clock signal (2 times the PN clock) is used to clock two bits of I and Q data into the bit 0 and bit 1 input of the I and Q correlators. The length of the correlators is set by loading the control register in the chip. The output from the correlators for the I and Q channels are 8-bit two's complement values that are scaled, formatted, and centered at the mid-point of the correlation output range. This value is output to the ACQR.

4-18.5.2 There is an NCO in each of the correlators. The NCO in the I channel correlator (designated as carrier NCO) is loaded by the DMDP and a 25-MHz clock is provided to clock the NCO to generate the nominal carrier frequency of 8.5 MHz. The NCO is updated based on the rising edge of the 20-kHz interrupt. The load pulse to the NCO is generated inside the correlator. The output of the NCO is converted to analog, low-pass filtered, and output on the J1 connector.

4-18.6 Timing Low-Pass Filter

The 8-bit output of the NCO in the Demod chip is the source of clocks used in the DMSS and throughout the IR. These eight bits are in 2's complement format. The sign bit is inverted and the signal is input to a DAC that converts the digital data to analog at the rate of 70 MHz. The output of the DAC is fed into a seven-section 1-dB passband ripple Chebyshev low-pass filter. The cutoff frequency of the filter is 28 MHz +/-500 kHz and the stop band attenuation is at least 40 db.

4-18.7 Carrier Low-Pass Filter

The 8-bit output of the NCO in the correlator chip is the carrier frequency. These eight bits are in 2's complement format. The sign bit is inverted and the signal is input to a DAC that converts the digital data to analog at the rate of 25 MHz. The output of the DAC is fed into a five-section 0.1-dB passband ripple Elliptic low-pass filter. The cutoff frequency of the filter is 9.5 MHz +/-500 kHz and the stop band attenuation is at least 45 dB.

4-18.8 Clock Generation

The output of the timing low-pass filter is converted back to digital using a zero crossing detector. In non-spread mode, this clock is used to provide the system clock. In spread mode, the PN clock signal is used as the system clock. The PN clock can be either the tracking sample clock or the acquisition sample clock. The clock selection is performed based on the mode by the TMS. The system clock is input to the Demod chip and is divided down to provide all clocks required in the chip and board.

4-19 RF Downconverter No. 2

4-19.1 Refer to figure 4-18 for the following RFDC2 functional description. RFDC2 accepts a 370-MHz IF return service input and sends it to a bandpass filter, to a front panel test point, and to the HRDC. The nominal input 370-MHz IF signal is bandpass filtered and downconverted to a nominal 70-MHz IF through the first downconversion process. Estimated Doppler-induced frequency errors, based on available ephemeris data, are removed during this initial downconversion process under control of the digital processing portion of the IR, through Doppler-based frequency commands periodically provided for control of the 300-MHz NCO downconversion signal. The nominal 70-MHz IF signal passes through an LPF and RF amplifier before input to an RF switch. The RF switch also accepts a 70-MHz test input from the SYNTH. TIME provides the control signal determining which signal is passed. The selected 70-MHz signal is applied to a 4-way bandpass filtering network with selectable bandwidths of 0.25, 4, 8, and 16 MHz. TIME provides the bandpass filtering selection control signals.

4-19.2 The filtered 70-MHz IF output is split, with one portion output to RFDC1 and the other input to

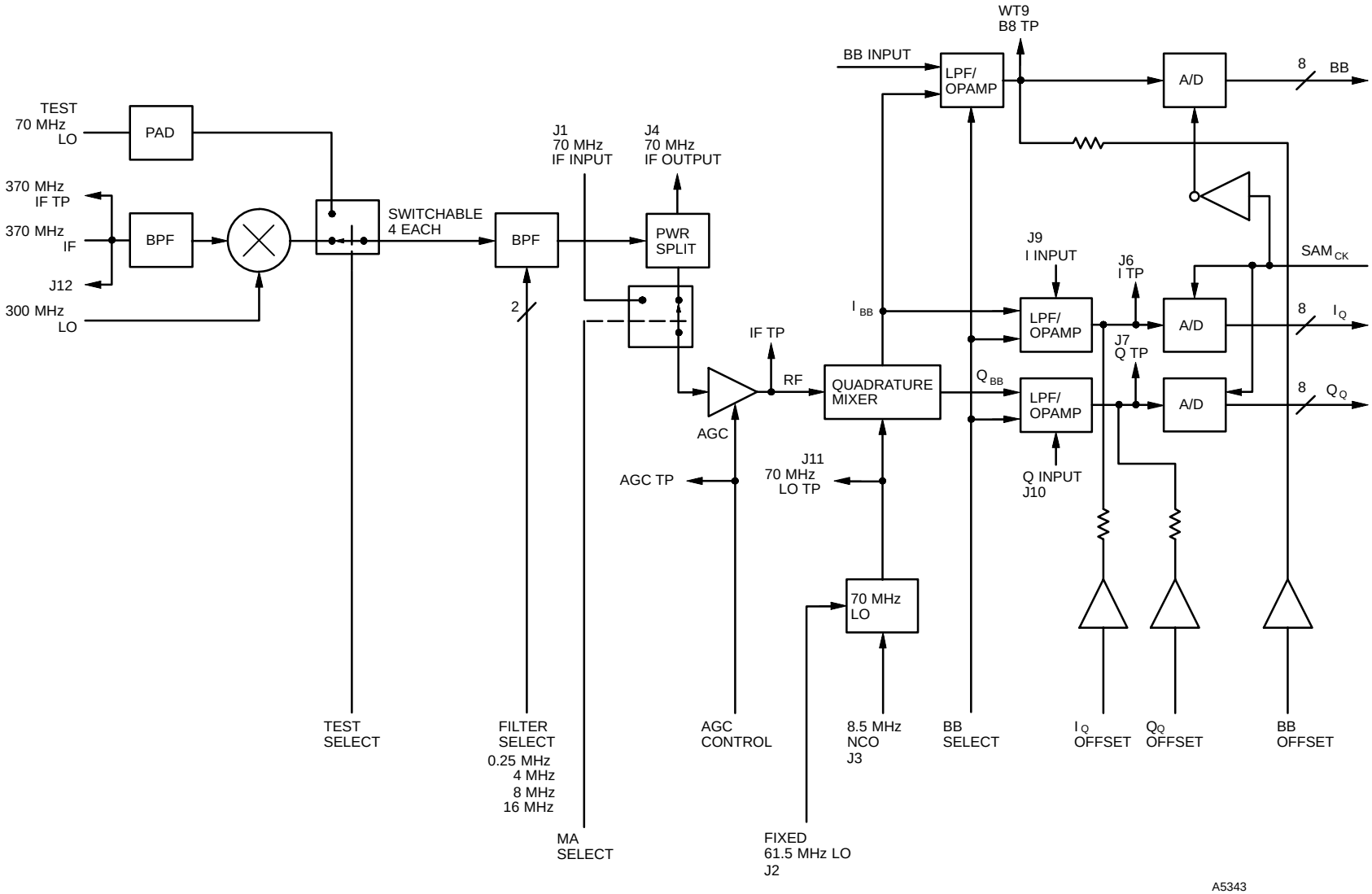


Figure 4—18. RFDC2 Functional Block Diagram

an RF switch that also accepts a 70-MHz IF signal from RFDC1. The selected 70-MHz IF signal passes through an AGC controlled variable attenuator. The AGC signal is developed by the digital processing portion of the IR (DMDP) based on signal-plus-noise measurements, with the AGC operating point set to avoid excessive saturation of the A/D converter in RFDC2. A tap-off of the AGC input is provided at the maintenance panel. The IF-filtered, AGC-amplified 70-MHz signal is downconverted to baseband I and Q analog signals by an I/Q mixer. The 70-MHz IF signal is also output as a test point. The I/Q mixer also accepts a 70-MHz LO signal that is developed from an 8.5-MHz NCO input from the DMSS (Q) and a fixed 61.5-MHz LO from the SYNTH. The 8.5-MHz NCO input is synchronized to the carrier and provides the closed-loop signal processing function necessary for proper data recovery.

4-19.3 The resultant outputs from the I/Q mixer are quadrature baseband (QBB) and inphase baseband (IBB) components of the original IF input. The baseband components are low pass filtered and then input to separate Inst. Amps which also accept a similar baseband component signal from HRDC via test points on top of RFDC2. The IBB component is also routed to a third Inst. Amp circuit which accepts a high-rate baseband (BB) downconversion of the high-data rate IF signal from the HRDC. The selected baseband signals IBB and QBB are output to RFDC1 and all three (IBB, QBB, and BB) are applied to separate A/D converters. The A/D converters utilize the sample clock from the DMSS (Q) as the sampling rate during the conversion process. The rate varies depending on the IR configuration with the sample clock less than or equal to 25 MHz. Prior to input to the A/D converters, the selected baseband component signals are offset depending on the noncoherent AGC function of the DMDP. The output of the A/D converter consists of 8-bits of baseband component data at the sample rate and are output to DMSS (Q).

4-20 Synthesizer

Refer to figure 4-19 for the following SYNTH functional description. SYNTH accepts a 10-MHz reference signal from an external interface and splits it with one portion output to a test point on the maintenance panel and the other for internal processing. The 10-MHz signal is sent through a BPF with a center frequency of 10 MHz and a bandwidth of 1 MHz. The filtered signal is buffered and split with one portion for status monitoring and the other for further processing in a 140-MHz PLL. The 140-MHz PLL is performed by taking the output of a 140-MHz VCXO and dividing it by fourteen. The resultant 10-MHz signal is phase detected with the 10-MHz reference input. The phase error signal is put through a loop filter which drives the 140-MHz VCXO. SYNTH produces the following clocks and timing signals:

a. A 70-MHz LO signal is produced by dividing the 140-MHz phase locked signal by two.

b. A 300-MHz LO is produces by upconverting the 20-MHz NCO input using a 280-MHz signal. The 280-MHz signal is produced by multiplying the 140-MHz signal by two.

c. A 50-MHz clock is produced by adding the 20-MHz NCO input and the 10-MHz output of the divide by fourteen network in the 140-MHz PLL. The resultant 30-MHz signals has a 50-MHz harmonic present which is 10 dB below the 30-MHz signal. A 50-MHz filter is used to reject the undesirable signals leaving the 50-MHz component.

d. A 61.5-MHz LO and 61.5-MHz clock are produced by high side downconverting the 61.5-MHz VCXO to 8.5-MHz using a 70-MHz produced signal. The 70-MHz signal is produced by dividing the 140-MHz PLL signal by two. The 8.5-MHz signal passed through a bandpass filter (8-MHz bandwidth) and then divided by 17 to produce 0.5 MHz. The 0.5-MHz downconversion signal which is phase compared a 0.5 MHz signal which is produced by dividing the 10-MHz (from the 140-MHz PLL) by 20. The resulting phase error output is then put through a loop filter which drives the 61.5-MHz VCXO.

e. SYNTH produces an 8.5-MHz output signal which is a direct tap-off of the 8.5-MHz signal produced in the 61.5-MHz PLL.

f. The variable 61.5-MHz LO output is produced by subtracting 8.5-MHz NCO input

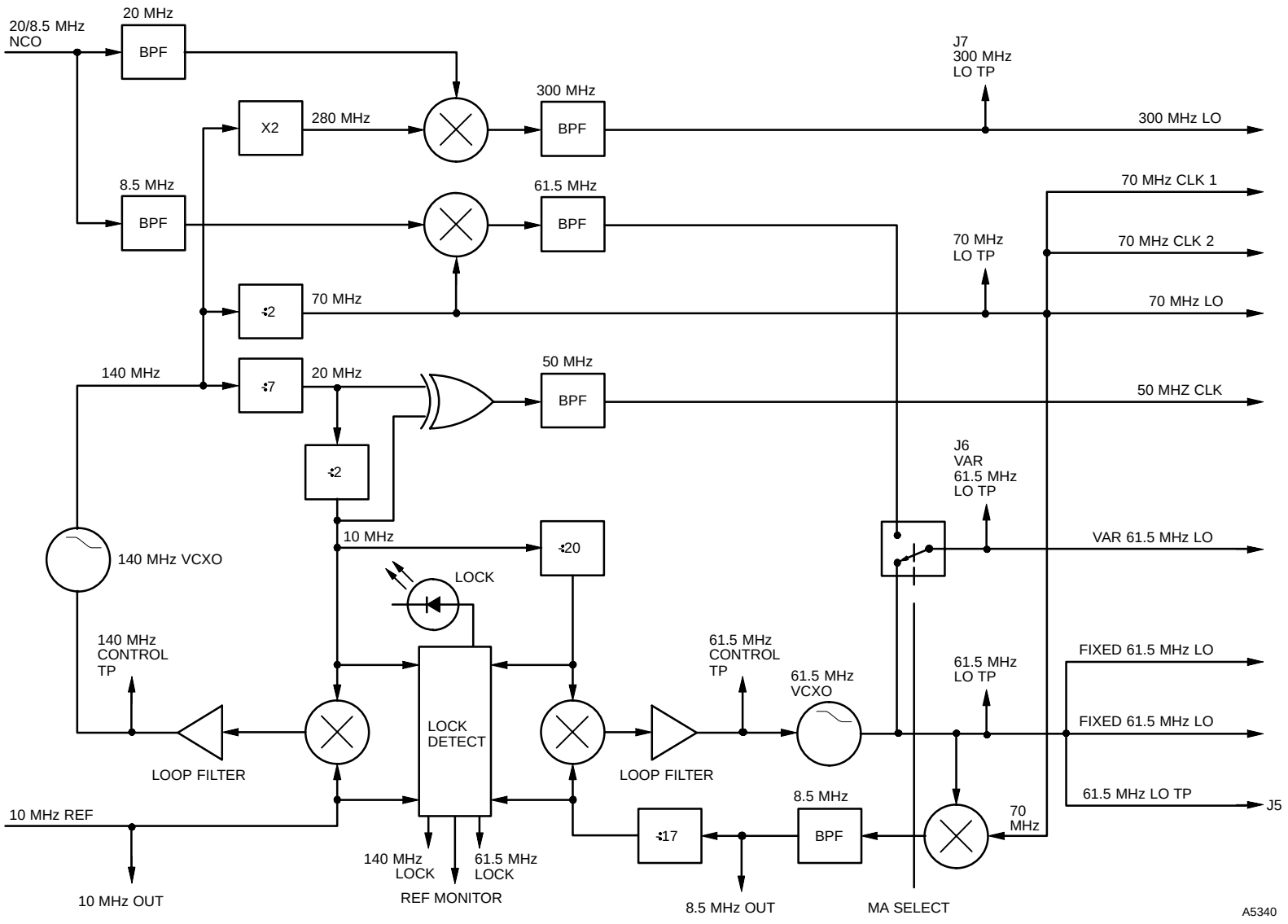


Figure 4—19. SYNTH Functional Block Diagram

from the internally generated 70-MHz signal. The 70-MHz signal is produced by dividing the 140-MHz PLL signal by two.

g. SYNTH provides status by two means: (1) an LED mounted on the PWA which turns on to indicate the 61.5-MHz PLL, 140-MHz PLL, and 10-MHz reference input are correct, and (2) three output status lines indicating the same.

4-21 RF Downconverter No. 1

4-21.1 Refer to figure 4-20 for the following RFDC1 functional description. RFDC1 accepts an 8.5-MHz IF input and an 8.5-MHz IF test input that are applied to an RF switch. The TIME provides the control signal to the RF switch. The selected 8.5-MHz IF signal passes through a variable attenuator that is controlled by on-board AGC that is derived from the two most significant bits (MSB) of the I and Q sample data. The gain control is sufficient to allow the AGC to keep the change in level for the baseband input to the analog/digital converters to less than +/-1dB for the specified input range of the 8.5-MHz IF input. The gain controlled signal is then upconverted to 70-MHz by mixing it with a fixed 61.5-MHz LO signal (during non-MA configurations) or a variable 61.5-MHz LO signal (during MA configurations) from the SYNTH. Estimated Doppler-induced frequency errors, based on available ephemeris data, are removed during this upconversion process under control of the digital processing portion of the IR, through Doppler-based frequency commands periodically provided for control of the 61.5-MHz NCO input signal.

4-21.2 The 70-MHz IF signal is applied to an anti-alias bandpass filter with a center frequency of 70 MHz and a bandwidth of 8 MHz. The filtered output is split, with one portion output to RFDC2 and the other input to an RF switch that also accepts a 70-MHz IF signal from RFDC2. The selected 70-MHz IF signal passes through a variable attenuator that is controlled by the same AGC signal used to control the 8.5-MHz IF input. Both AGC variable attenuators are controlled by the digital processing portion of the RFDC1 based on signal-plus-noise measurements at the analog-to-digital (A/D) output, with the AGC operating point set to avoid excessive saturation of the A/D converter. The gain controlled 70-MHz signal is then applied to an I/Q mixer circuit and also output as a test point. The I/Q mixer also accepts a 70-MHz LO signal that is developed from an 8.5-MHz NCO input from the DMSS (I) and a fixed 61.5-MHz LO from the SYNTH. The 8.5-MHz NCO input is synchronized to the carrier and provides the closed-loop signal processing function necessary for proper data recovery.

4-21.3 The resultant outputs from the I/Q mixer are quadrature baseband (QBB) and inphase baseband (IBB) components of the original IF input. The baseband components are low pass filtered and then input to separate Inst. Amps which also accept a similar baseband component signal from RFDC2. The selected baseband signal has a tap-off for a test point and applied to an A/D converter. The A/D converter utilizes the sample clock from DMSS (I) as the sampling rate during the conversion process. The rate varies depending on the IR configuration with the sample clock being less than or equal to 25 MHz. Prior to input to the A/D converters, the selected baseband component signals are offset depending on the noncoherent AGC function of the DMDP. The output of the A/D converter consists of 8-bits of baseband component data at the sample rate and are output to DMSS (I). As mentioned earlier, the two MSBs are used to develop the internal AGC level.

4-22 Touch Panel Display

Refer to figure 4-21 for the following touch panel display functional description. The touch panel display scans the front panel switch rows until either a serial input is received or a switch closure is detected. If a serial input is received, switch scanning is suspended until the input is processed. If a switch closure is detected, then the closed row number is stored in a register and the columns are scanned to find the closed column. The data is then sent to the MCP.

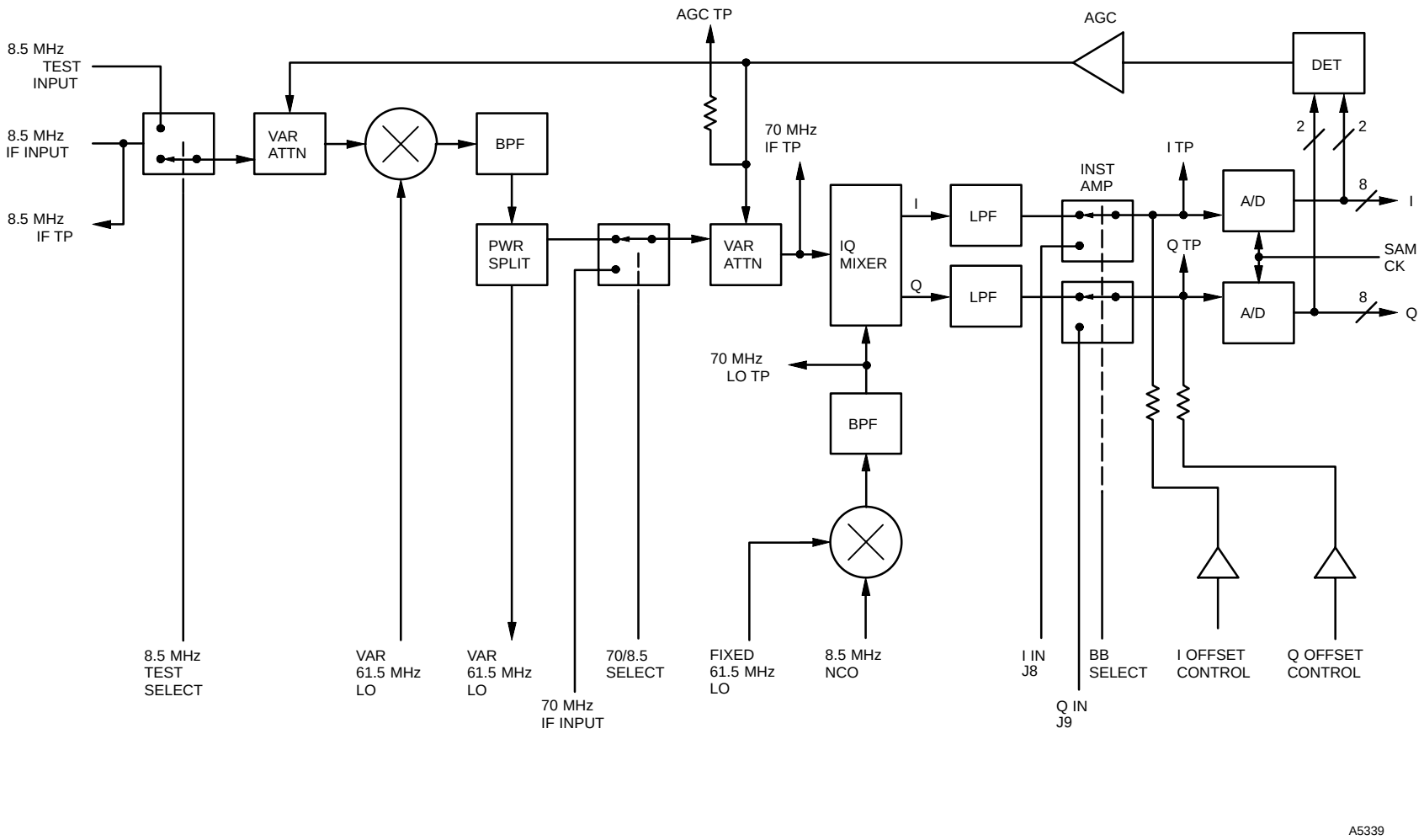


Figure 4—20. RFDC1 Functional Block Diagram

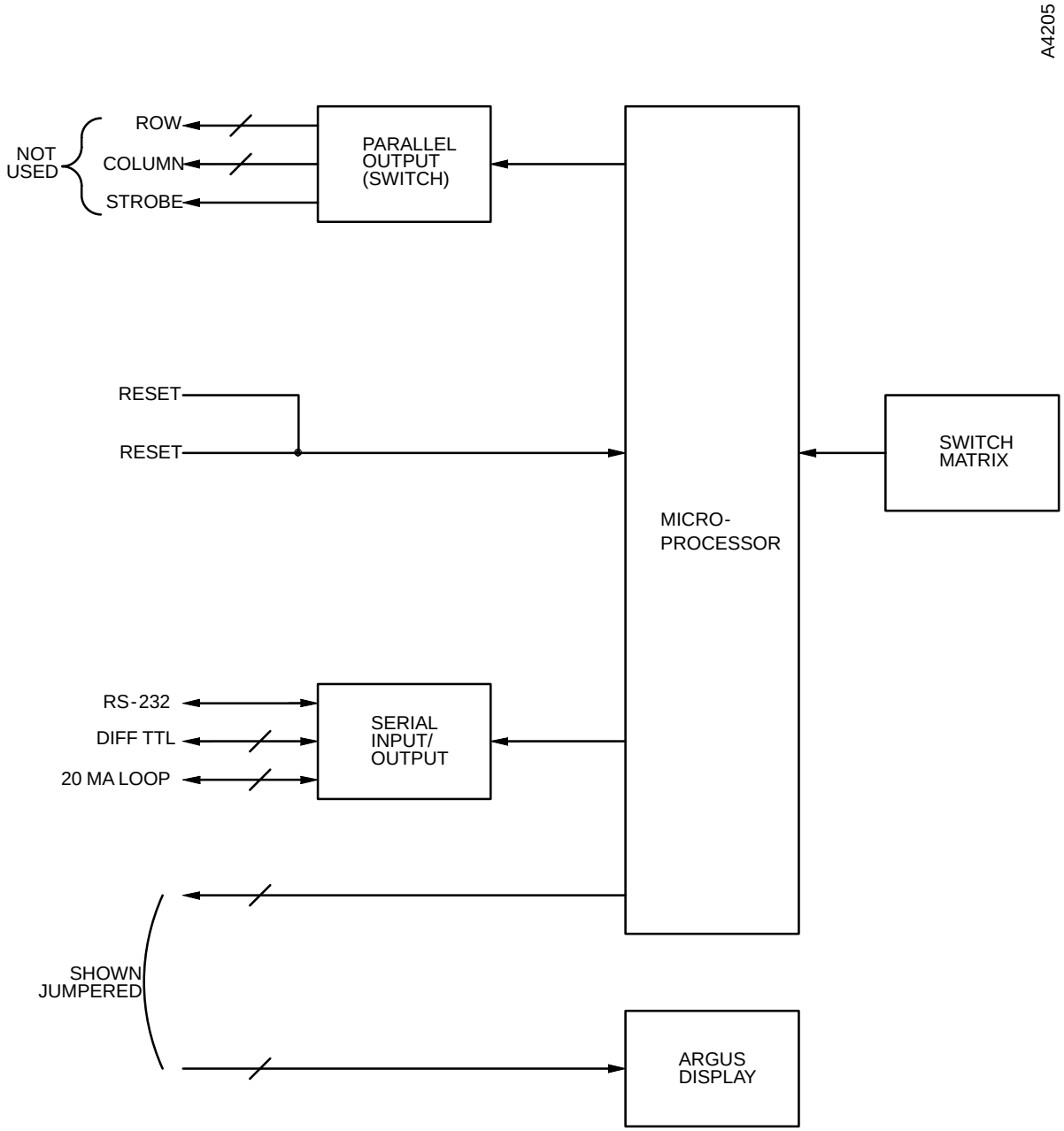


Figure 4—21. Touch Panel Display Functional Block Diagram

4-22.1 Switch Matrix

The switch matrix is composed of infrared emitter/sensor pairs. These pairs are on opposite edges of the display (side to side and top to bottom). Scanning starts by turning on an emitter and enabling its corresponding sensor. If the sensor receives the emitter signal, the switch is not closed and scanning proceeds to the next emitter/sensor pair. A microprocessor controls the switch overlay and serial communications (which include display inputs and switch outputs). In the serial mode, data first goes to the microprocessor and is then converted to a parallel format before being sent to the display. Conversely, in the parallel mode, ASCII data is sent directly to the display input port and switch data comes from the microprocessors's parallel output. This is why it is necessary to have a jumper cable installed for serial operation and removed for parallel operation.

4-22.2 Switch Selectable Options

Many of the switches used to select options are read only on power-up and reset. It is therefore required that after changing any switch setting, a power-up or reset must be initiated. In some cases (e.g., single touch/multi-touch) the switch settings become power-up default conditions for software alterable functions.

4-22.3 Blanking/Dimming

The touch panel display has a combination blanking/dimming input. It can be used for blanking, dimming, both, or neither. For no blanking or dimming, no connection is to be made to the input. For dimming only, connect a 25K potentiometer in series with a 1.5K resistor between VCC (+5 Vdc) and the blanking/dimming input. Maximum brightness occurs when maximum resistance is in the circuit. For blanking only, place a 1K resistor between VCC and the blanking/dimming input. For a combination, connect both circuits previously mentioned.

4-22.4 Reset

Holding this input to a low for a minimum of 20 milliseconds resets the unit to its initial condition and loads all DIP switch settings into the touch panel display controller.

4-22.5 Test Switch

The test switch on SW1 must be OFF at all times. If left ON, switch matrix scanning continues despite interruption of an infrared beam. This switch is used only for testing and set-up.

4-22.6 Switch Output

Switch ME1 controls the switch output offset. With ME1 in the OFF position, row data is output as rows 0 thru 11, column data is output as 0 thru 19. When ME1 is in the ON position, row data is output as 1 thru 12, column data as 1 thru 20. ME2 controls how many switch position can be touched at the same time. ME2 in the OFF position inhibits output switch data when two or more touch switch position are closed at the same time. ME2 in the ON position allows the first scanned switch to be output when two or more are closed at the same time.

4-22.7 Beeper

The beeper is enabled by placing the BP switch in the OFF position. The beeper is disabled when the BP switch is in the ON position. After the beeper is enabled, it beeps when a switch closure is detected or when an ASCII 07 (BEL) is sent in the serial mode.

4-22.8 Self Test

A partial self test is enabled by placing a jumper wire from pin 2 to pin 3 of the serial connector (J2). With this jumper installed, a closed switch position is displayed on the display in the following format: "@, 2-character row number, 2-character column number." For example, if ME1 is ON and the top row, left column switch is closed, the unit display "@0101". A closed switch at the bottom row, left column displays "@1201".

4-23 High-Rate Downconverter

4-23.1 HRDC (used only in KSA configurations) accepts a high-rate data 370-MHz IF return service input signal (see figure 4-22) and sends it to a set of amplifiers and AGC controlled variable attenuator. The variable attenuator is controlled by on-board AGC that is derived from the baseband analog processed signal that is compared to a predetermined threshold level. The resultant signal is converted to a dc voltage level (0 - 10.0 Vdc) and fed to the variable attenuator. The gain control is sufficient to allow the AGC to keep the change in level for the baseband input to the analog/digital converters in RFDC2 to less than +/-1 dB for the specified input range of the 370-MHz IF input. The gain controlled signal is then applied to a 4-way bandpass filtering network with selectable bandwidths of 30.0, 48.0, 76.0, and 120.0 MHz. TIME provides the bandpass filtering selection control signals.

4-23.2 The IF-filtered, AGC-amplified 370-MHz signal (see figure 4-23) is downconverted to baseband I and Q analog signals by an I/Q mixer. The 370-MHz IF signal is also output as a test point. The I/Q mixer also accepts a 370-MHz LO signal that is developed from a 300-MHz LO and a 70-MHz LO from the RFDC2. Estimated Doppler-induced frequency errors, based on available ephemeris data, are removed during this downconversion process under control of the digital processing portion of the IR, through Doppler-based frequency commands periodically provided for control of the 300-MHz NCO downconversion signal from RFDC2. The 70-MHz NCO input is synchronized to the carrier and provides the closed-loop signal processing function necessary for proper data recovery. The resultant outputs from the I/Q mixer are quadrature baseband

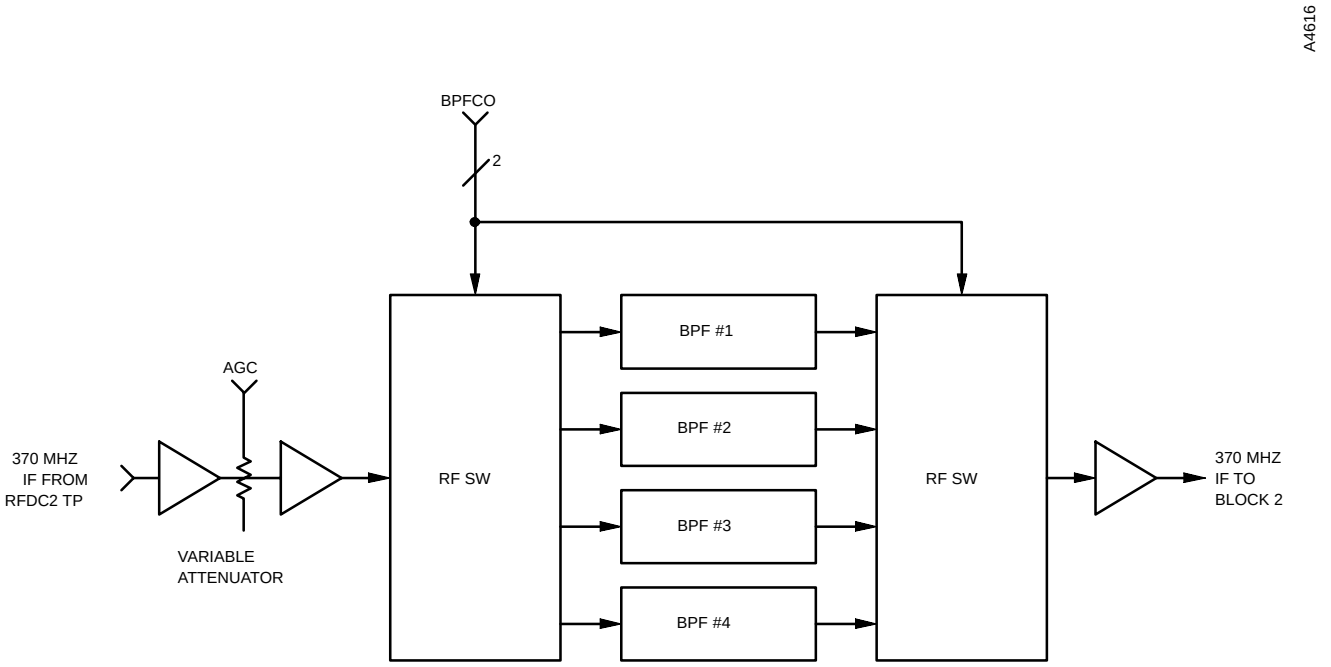


Figure 4—22. HRDC Front End Functional Block Diagram

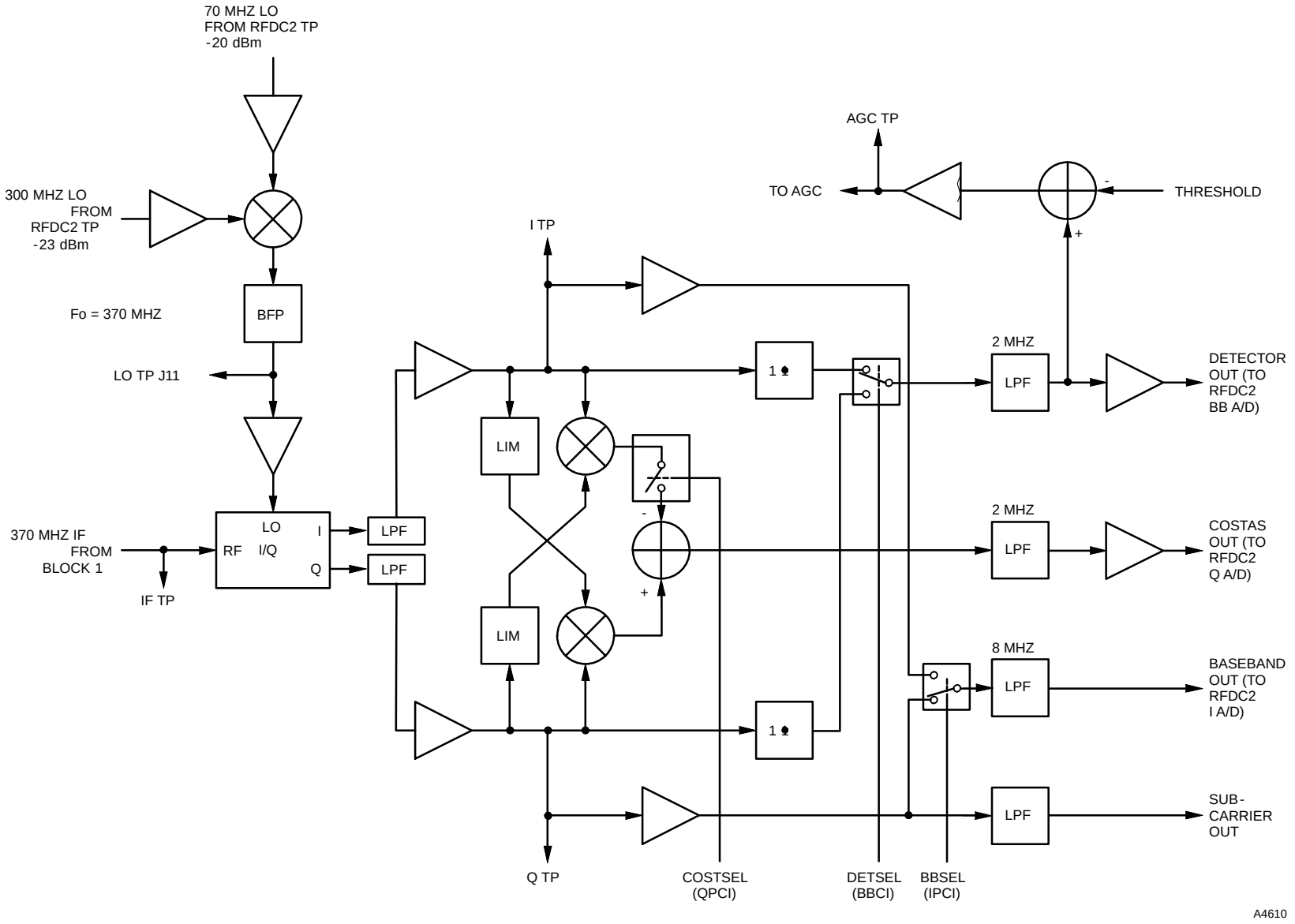


Figure 4—23. HRDC RF Downconversion Section Functional Block Diagram

(QBB) and inphase baseband (IBB) components of the original IF input. The baseband components are low pass filtered and amplified prior to being input to either the COSTAS circuitry, detector circuitry, or the baseband output circuitry. All three processing circuits output their selected outputs to RFDC2 for further IR signal processing.

4-24 Integrated Receiver External Interface Description

Refer to table 4-1 for a description and connector pin identification of the external interfaces for the Integrated Receiver.

4-25 Integrated Receiver Internal Interface Description

During Level 1 maintenance, the only accessible internal interface signals are located on the maintenance panel and described in section 3, table 3-2. Descriptions of the remaining internal interface signals are not applicable to Level 1 maintenance; therefore, this paragraph is not applicable.

4-26 Mechanical Components

This paragraph is not applicable to the Integrated Receiver.

Table 4—1. External Interface Signals

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J101	A B C	115VAC CHASSIS GND 115VAC RTN	Site—supplied source power.
J102	1 2	8.5 MHz SHIELD	8.5—MHz subcarrier signal input used during KSA and MA return service configurations.
J103	1 2	370 MHz IF SHIELD	370—MHz IF signal used during KSA and SSA return service configurations.
J104	1 2	10 MHz CTFS SHIELD	Common Time and Frequency System (CTFS) reference input signal used to synchronize the IR's 140—MHz VCXO.
J105	1 2	1PPS CTFS SHIELD	CTFS reference time mark used to synchronize the IR's 50—MHz clock.
J106	1 2	TOY CTFS SHIELD	CTFS unmodulated IRIG—B (time of year) data signal.
J107	1 2 14	DSUD+ DSUD— SHIELD	Differentially driven output of selected I or single user data. Used during KSA, SSA, and MA configurations.
	3 4 16	DSUC+ DSUC— SHIELD	Differentially driven reference clock for the selected I or single user data output. Data is valid on the rising edge of the clock.
	5 6 18	QD+ QD— SHIELD	Differentially driven output of selected Q data. Used during KSA, SSA, and MA configurations.
	7 8	QC+ QC—	Differentially driven reference clock for the selected Q data output. Data is valid on the rising edge of the clock.
	10 23 11 24 12 25 13	RTA0 RTA1 RTA2 RTA3 RTA4 RTAP RTAR	1553 Bus IR remote terminal address select inputs.

Table 4—1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J108	1 2 9	IPN+ IPN— SHIELD	Recovered DG—1 mode 1/2 inphase pseudorandom—noise digital code data processed during MA configuration for the MA beamforming equipment.
	10 11 3	QPN+ QPN— SHIELD	Recovered DG—1 mode 1/2 quadrature pseudorandom—noise digital code data processed during MA configuration for the MA beamforming equipment.
	4 5 12	IPNC+ IPNC— SHIELD	Recovered DG—1 mode 1/2 inphase pseudorandom—noise digital code data clock processed during MA configuration for the MA beamforming equipment.
	13 14 6	QPNC+ QPCN— SHIELD	Recovered DG—1 mode 1/2 quadrature pseudorandom—noise digital code data clock processed during MA configuration for the MA beamforming equipment.
	7 8 15	PNLOCK+ PNLOCK— SHIELD	PN lock status signal where a logic 1 signifies synchronization of the PN code has been achieved.
J109	19 20 1	ICIDO+ ICIDO— SHIELD	Differential input baseband demodulated sign—magnitude I combining signal (bit 0) from a second co—located IR. Used during SSA configuration.
	2 3 21	ICID1+ ICID2— SHIELD	Differential input baseband demodulated sign—magnitude I combining signal (bit 1) from a second co—located IR. Used during SSA configuration.
	22 23 4	ICID2+ ICID2— SHIELD	Differential input baseband demodulated sign—magnitude I combining signal (bit 2) from a second co—located IR. Used during SSA configuration.
	5 6 24	ICID4+ ICID4— SHIELD	Differential input baseband demodulated sign—magnitude I combining signal (bit 3) from a second co—located IR. Used during SSA configuration.
	25 26 7	ICID4+ ICID4— SHIELD	Differential input baseband demodulated sign—magnitude I combining signal (bit 4) from a second co—located IR. Used during SSA configuration.
	8 9 27	ICIC+ ICIC— SHIELD	Differential input I combining reference clock for I combining input data. The data is valid on the rising edge of clock.

Table 4—1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J109 (Cont'd)	28 29 10	QCID0+ QCID1— SHIELD	Differential input baseband demodulated sign—magnitude Q combining signal (bit 0) from a second co—located IR. Used during SSA configuration.
	11 12 30	QCID1+ QCID1— SHIELD	Differential input baseband demodulated sign—magnitude Q combining signal (bit 1) from a second co—located IR. Used during SSA configuration.
	31 32 13	QCID2+ QCID2— SHIELD	Differential input baseband demodulated sign—magnitude Q combining signal (bit 2) from a second co—located IR. Used during SSA configuration.
	14 15 33	QCID3+ QCID3— SHIELD	Differential input baseband demodulated sign—magnitude Q combining signal (bit 3) from a second co—located IR. Used during SSA configuration.
	34 35 16	QCID4+ QCID4— SHIELD	Differential input baseband demodulated sign — magnitude Q combining signal (bit 7) from a second co—located IR. Used during SSA configuration.
	17 18 36	QCIC+ QCIC— SHIELD	Differential input Q combining reference clock for Q combining input data. The data is valid on the rising edge of clock.
J110	19 20 1	ICOD0+ ICOD0— SHIELD	Differential output baseband demodulated sign—magnitude I combining signal (bit 0) for a second co—located IR. Used during SSA configuration.
	2 3 21	ICOD1+ ICOD1— SHIELD	Differential output baseband demodulated sign—magnitude I combining signal (bit 1) for a second co—located IR. Used during SSA configuration.
	22 23 4	ICOD2+ ICOD2— SHIELD	Differential output baseband demodulated sign—magnitude I combining signal (bit 2) for a second co—located IR. Used during SSA configuration.
	5 6 24	ICOD3+ ICOD3— SHIELD	Differential output baseband demodulated sign—magnitude I combining signal (bit 3) for a second co—located IR. Used during SSA configuration.
	25 26 7	ICOD4+ ICOD4— SHIELD	Differential output baseband demodulated sign—magnitude I combining signal (bit 4) for a second co—located IR. Used during SSA configuration.

Table 4—1. External Interface Signals (Continued)

CONNECTOR	PIN	MNEMONIC	DESCRIPTION
J110 (Cont'd)	8 9 27	ICOC+ ICOC— SHIELD	Differential output I combining reference clock for I combining output data. The data is valid on the rising edge of clock.
	28 29 10	QCOD0+ QCOD0— SHIELD	Differential output baseband demodulated sign—magnitude Q combining signal (bit 0) for a second co—located IR. Used during SSA configuration.
	11 12 30	QCOD1+ QCOD1— SHIELD	Differential output baseband demodulated sign—magnitude Q combining signal (bit 1) for a second co—located IR. Used during SSA configuration.
	31 32 13	QCOD2+ QCOD2— SHIELD	Differential output baseband demodulated sign—magnitude Q combining signal (bit 2) for a second co—located IR. Used during SSA configuration.
	14 15 33	QCOD3+ QCOD3— SHIELD	Differential output baseband demodulated sign—magnitude Q combining signal (bit 3) for a second co—located IR. Used during SSA configuration.
	34 35 16	QCOD4+ QCOD4— SHIELD	Differential output baseband demodulated sign—magnitude Q combining signal (bit 4) for a second co—located IR. Used during SSA configuration.
	17 18 36	QCOC+ QCOC— SHIELD	Differential output Q combining reference clock for Q combining output data. The data is valid on the rising edge of clock.
J111	A B C	1553 BUS 1553 BUS RTN SHIELD	MIL—STD—1553B digital time division command/response multiplex data bus (A1).
J112	A B C	1553 BUS 1553 BUS RTN SHIELD	MIL—STD—1553B digital time division command/response multiplex data bus (A2).
J113	A B C	EE EER SHIELD	Error envelope analog 12 volts p—p (maximum) output of the KSA Autotrack function.
J114	A B C	CLS CLR SHIELD	Carrier lock status digital signal where a logic 1 signifies the carrier has been phase locked by the DMDP.

Section 5 — Maintenance

5—1 Introduction

This section contains information to aid personnel in the Level 1 maintenance of the Integrated Receiver. Level 1 maintenance is defined as those tasks permitting a technician (with the unit installed in the equipment rack) to fault isolate a failure to the chassis line replaceable unit (LRU), remove and replace the faulty LRU, and restore the unit to operation within a specified time. Major component LRUs are listed in table 5-1. Before performing any procedures, refer to paragraph 3-5 for warnings aimed at preventing death or injury and equipment damage.

Level 2 maintenance instructions are not provided for in this manual. Level 2 maintenance is defined

Table 5—1. Replaceable LRUs

NOMENCLATURE	PART	LRU	LEVEL
Integrated Receiver	7472100		
Timing Generator	7473000-502	X	1, 2
Demodulator/Symbol Synchronizer	7473100-502	X	1, 2
Acquisition Processor	7473200-501	X	1, 2
PN Processor	7473300-501	X	1, 2
Output Processor	7473400-502	X	1, 2
Modem Control Processor	7473600	X	1, 2
RF Downconverter No. 1	7474000-500	X	1, 2
RF Downconverter No. 2	7474300-500	X	1, 2
Synthesizer	7474600-500	X	1, 2
Demodulator Processor	7476100	X	1, 2
Power Supply No. 1	LFQ-27-1	X	1, 2
Power Supply No. 2	RMV223B-2330-0450	X	1, 2
Power Supply No. 3	7516900	X	1, 2
High Rate Downconverter	7510500	X	1, 2
Tubeaxial Fan	A47-B15A-15T3-000	X	1, 2
Lamp Cartridge (green, DS1 only)	CF296CWPG6-120VAC-B	X	1, 2
Lamp Cartridge (green)	507-4857-3732-500	X	1, 2
Lamp Cartridge (red)	507-4757-3731-500	X	1, 2
Lamp Cartridge (amber)	507-4957-3733-500	X	1, 2
Touch Panel Display	7519500	X	2
Lampholder	DH0-30Y-D86BWC	X	2
Pushbutton Switch	W403PGR	X	2
Toggle Switch (AC POWER)	MS24659-22F	X	2
Toggle Switch (LOCAL/REMOTE)	MS24658-23F	X	2
Circuit Breaker	MS25244-10	X	2
RF Coaxial Switch	8021-A35-A4B-ICO	X	2
Harness Assembly	7472160	X	2

as those tasks permitting a technician (with the unit removed from the equipment rack and taken to the HMD area) to fault isolate the failure to the LRU. Repairable LRUs are sent to the depot for repair. Depot level maintenance consists of repairing failed LRUs to the piece part, repairing any other discrepancy not discovered at the Level 1/2 maintenance level, equipment refurbishment and performing major modifications to the equipment, when required. The IR manufacturer maintains depot maintenance facilities for all LRUs. Refer to table 5-2 for the IR maintenance concept.

5—2 Performance Standards

Minimum performance standards for Level 1 operation and maintenance are detailed in paragraph 5-6 operational verification. If the IR fails to meet any of the procedural performance steps, perform IR fault isolation procedures (paragraph 5-4).

Table 5—2. Maintenance Concept

LEVEL 1 MAINTENANCE	LEVEL 2 MAINTENANCE	DEPOT LEVEL
TASK	TASK	TASK
* Detect malfunctions	* Localize fault to subassembly	* Repair LRUs
* Isolate LRU	* Isolate LRU	
* Remove/replace LRU	* Remove/replace LRU	
* Preventive maintenance	* Preventive maintenance	
Timing Generator		Repair
Demodulator/Symbol Synchronizer		Repair
Acquisition Processor		Repair
PN Processor		Repair
Output Processor		Repair
Modem Control Processor		Repair
RF Downconverter No. 1		Repair
RF Downconverter No. 2		Repair
Synthesizer		Repair
Demodulator Processor		Repair
Power Supply No. 1		Repair
Power Supply No. 2		Repair
Power Supply No. 3		Repair
High Rate Downconverter		Repair
Lamp Cartridges (all) - Discard		
Tubeaxial Fan - Discard		
	Harness Assembly	Repair
	Touch Panel Display	Repair
	Lampholders (all) - Discard	
	Front Panel Switches - Discard	
	Circuit Breaker - Discard	
	RF Coaxial Switch - Discard	

5—3 Test and Adjustment Procedures

Test and adjustment procedures for the IR include only power supply adjustments. The following procedure describes how to adjust PS1 and PS2.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

d. Applying pressure to bottom cover toward unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

e. Carefully lower bottom panel to gain access to power supplies.

f. Refer to the following list of voltage adjustments and figures 5-1 and 5-2 for location of adjustment potentiometers when performing power supply voltage adjustments.

Power Supply	Adjustment	Test Point	Voltage
PS1	V-ADJ#1	+5	+5.0 +/-.25 Vdc
PS1	V-ADJ#2	+15	+15.0 +/-.5 Vdc
PS1	V-ADJ#3	-15	-15.0 +/-.5 Vdc
PS1	V-ADJ#4	+5RF	+5.0 +/-.25 Vdc
PS2	V1	-5.2	-5.2 +/-.25 Vdc
PS2	V2	+12	+12.0 +/-.25 Vdc
PS2	V3	-12	-12.0 +/-.25 Vdc

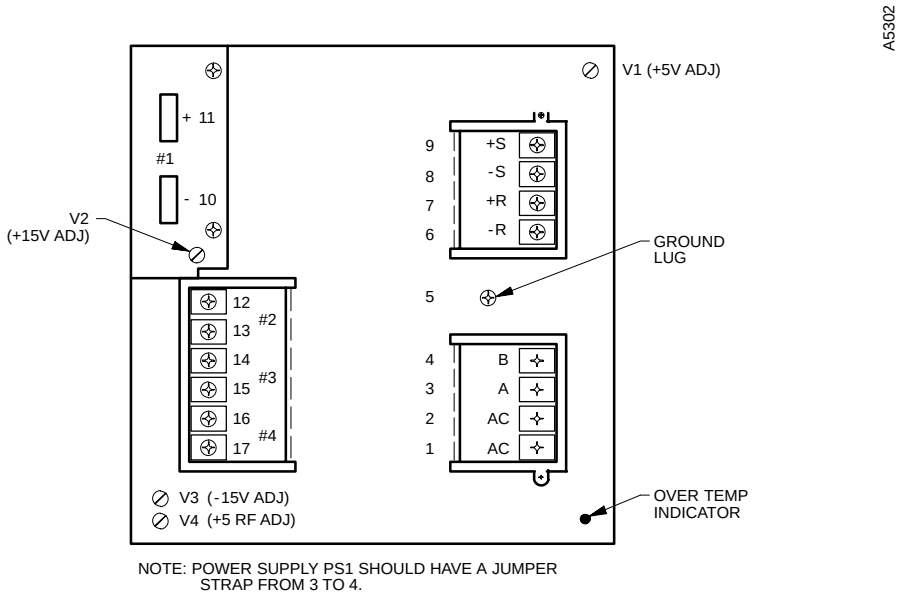


Figure 5—1. Power Supply No. 1 Voltage Adjustments

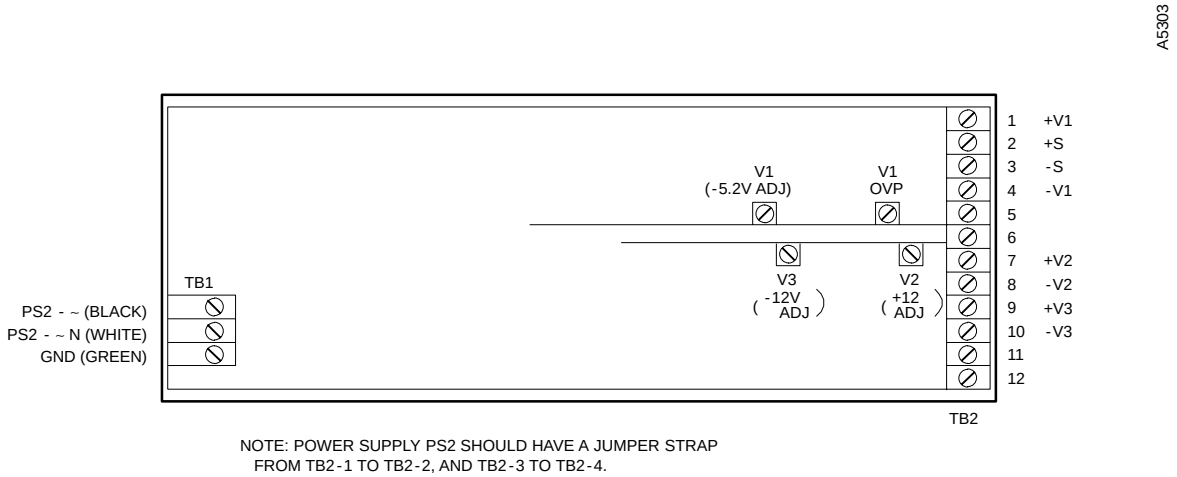


Figure 5—2. Power Supply No. 2 Voltage Adjustments

WARNING

When adjusting voltages, beware of power terminals. Voltage present may cause DEATH or injury.

g. Set AC POWER ON/OFF switch to ON.

h. Connect digital voltmeter to respective power supply voltage test point on the maintenance panel and adjust voltage to within specifications. If specifications cannot be achieved, replace faulty power supply and repeat this procedure.

i. Set AC POWER ON/OFF switch to OFF.

j. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

k. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

l. Tighten four front-panel captive screws to the cabinet assembly.

m. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

5—4 Fault Isolation (Troubleshooting)

Information to aid fault isolation within the IR to an LRU is presented in table 5-3. This procedure is performed at the unit level with the IR LOCAL/REMOTE switch set to the LOCAL position. Before performing any procedures, refer to paragraph 3-5 for safety information. Procedures for troubleshooting the IR may be used in conjunction with troubleshooting procedures in the respective O&M manuals (see section 3,

paragraph 3-11). If an LRU in the IR is faulty, refer to paragraph 5-7 for removal/replacement (R/R) procedures. The line maintenance technician (LMT) replaces the faulty LRU with a spare and sends the faulty assembly to the HMD for fault verification prior to shipment to the manufacturer for depot repair.

WARNING

Before attempting to perform any troubleshooting procedures, ensure that power has been removed (when possible) to prevent injury or DEATH from electric shock. It is recommended that at least two people are present at all times when working on energized equipment.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5—5 Preliminary Fault Isolation Steps

As a first step in fault isolation, perform the following preliminary steps. If any preliminary step leads to a possible fault, after correcting that possible fault, re-conduct paragraph 5-6 and verify that the fault(s) still exist.

a. Ensure all mechanical connections are secure. Check for improperly mated connectors, improperly seated PWAs, and evidence of physical damage.

b. Ensure power is available to unit.

c. Ensure (as nearly as possible) that all other equipment in, or associated with, the IR is operating properly.

d. Observe the front-panel display, indicators, and PWA LEDs for proper operation.

5—6 Operational Verification

This paragraph contains procedures that check-out and confirm the IR's Level 1 operational status while in local control. Before proceeding with any procedures involving the IR, refer to paragraph 3-5. Unless otherwise specified, all actions will take place from the IR front panel. Upon any step which does not give a normal indication, stop the operational verification procedure and proceed to table 5-3 and perform the fault isolation procedures.

a. Ensure paragraph 5-5, Preliminary Fault Isolation Steps has been completed in its entirety.

b. Place the ON/OFF switch to the OFF position.

c. Place the LOCAL/REMOTE switch to the LOCAL position.

d. Loosen the four captive screws holding the IR in the cabinet.

e. Slide the unit forward until the rail-guide locks are set to the locked position.

f. Using a flat-tipped screwdriver, loosen the four captive screws securing top cover to maintenance panel. Raise top cover to gain access to PWAs.

g. Place the ON/OFF switch to the ON position and verify the following:
   (1) AC POWER indicator turns on.
   (2) Cooling fan blowers turn on.
   (3) All seven DC POWER indicators turn-on.
   (4) Test indicator turns on.
   (5) All front-panel indicators turn on for a 1-second period.
   (6) All STATUS indicators are turned off (after item 5 above).

h. Verify the TEST indicator turns off after approximately 10 seconds, the FAULT indicator remains turned off, and the NORMAL indicator turns on.

i. Verify the MCP PWA RUN LED is turned on green.

j. Verify the Select Menu (figure 3-5) appears on the display. If not, select Previous Menu on display until Select Menu appears.

k. Select maintenance and verify the Maintenance Menu (figure 3-6) appears.

Table 5—3. Fault Isolation

STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
1.	Ensure ON/OFF switch is in the OFF position and the LOCAL/ REMOTE switch is in the LOCAL position.	All front-panel indicators are turned off.	Faulty power switch
2.	Loosen the front panel screws, slide the IR forward until rail-guide locks are set to locked position.		
3.	Loosen top-cover screws and raise top cover to gain access to PWAs.	All PWA indicators are turned off.	
4.	Place the ON/OFF switch to the ON position.	The AC POWER indictor turns on. The cooling fan blowers turn on. The DC POWER indicators turn on.	Site-power not available CB101 faulty POWER ON indicator/ lampholder faulty Faulty fan Faulty indicator/ lampholder Faulty power supply
5.	Using a digital multimeter, monitor dc power supply voltages at the maintenance panel.	See section 1, table 1-3.	Faulty power supply (Adjust if possible; see paragraph 5-3)
6.	Using an oscilloscope, monitor the 1PPS EXT test point at the maintenance panel.	See section 1, table 1-3.	Site-supplied 1PPS signal not available
7.	Using a frequency counter, monitor the 10 MHZ test point at the maintenance panel.	See section 1, table 1-3.	Site-supplied 10-MHz signal not available SYNTH PWA faulty

Table 5—3. Fault Isolation (Continued)

STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
8.	Using an oscilloscope, monitor the 1PPS INT at the maintenance panel.	Internally generated 1-Hz TTL signal with a 20% duty cycle.	SYNTH PWA faulty
9.	Press the RESET switch on maintenance panel.	The TEST indicator turns on and the NORMAL indicator turns off (except for 1-second test) for duration of the confidence BIT; the FAULT indicator remains turned off (except for 1-second test). At completion of the confidence BIT, the NORMAL indicator turns on and the TEST indicator turns off. The SELECT MENU is displayed.	Faulty indicator/ lampholder View the MCP PWA and replace the MCP PWA if the RUN LED is turned on RED. If after replacing the MCP PWA, this fault continues to occur, systematically replace each PWA on the VMEbus until the PWA with the VME fault is found. Replace display or display power supply (PS3) if display remains blank and the MCP PWA RUN indicator is turned on GREEN. View the Confidence and Online BIT Results displays (figures 3-11 and 3-12) and replace faulty PWA/LRU identified
10.	Select the Extended BIT Summary display (figure (3-7) and initiate the extended BIT processing. After all tests have completed, select Halt BIT and review LRU status (Tests 1-8 and Test 9)	The TEST indicator turns on and the NORMAL indicator turns off for duration of the extended BIT; the FAULT indicator remains turned off. At completion of the extended BIT, the NORMAL indicator turns on and the TEST indicator turns off.	A fault indication (FAULT indicator turned on and MCP PWA RUN indicator turned on red) may be induced by a failure in the ADPE interfaced to the 1553 bus View the Extended BIT Results displays (figures 3-8 and 3-9) and replace faulty PWA/LRU identified by the display status

Table 5—3. Fault Isolation (Continued)			
STEP	PROCEDURE	EXPECTED RESULTS	FAULT ANALYSIS
10.	(Continued)		View the MCP PWA and replace the MCP PWA if the RUN LED is turned on RED
11.	Perform Level 1 equipment group maintenance procedures to further isolate chassis fault.	Refer to applicable Level 1 O&M manual (see section 3, paragraph 3-11).	
12.	Replace chassis with good IR resident in STGT Electronics System Test Set (in the HMD area) if faulty LRU cannot be identified within Level 1 specified repair time.		

l. Select confidence test results and verify the Confidence Test Results display (figure 3-11) appears.

m. Verify a status of “GOOD” appears for all confidence tested LRUs.

n. Select Previous Menu; at the Maintenance Menu select the Display Firmware Version prompt.

o. Verify the Firmware Version display (figure 3-13) appears and the correct firmware versions are installed.

p. Select Previous Menu; at the Maintenance Menu select the display online BIT results.

q. Verify the Online BIT Results display (figure 3-12) appears and a status of “GOOD” appears next to all applicable online BIT tested LRUs.

r. Select Previous Menu; at the Maintenance Menu select Extended BIT Summary display.

s. Verify the Extended BIT Summary display (figure 3-7) appears; select Start BIT.

t. Select previous menu twice and verify the Select Menu appears.

u. At the Select Menu select configuration.

v. Verify the Configuration Menu (figure 3-19) appears.

w. At the Configuration Menu select the IR Service Config display.

x. Verify at the IR Service Config display (figure 3-20) that the operation mode is extended BIT and then at completion of test the mode returns to standby.

y. Select previous menu; at the Configuration display select the IR Demod Config display.

z. Select previous menu twice and verify the Select Menu appears.

aa. At the Select Menu, select maintenance and verify the Maintenance Menu appears.

ab. At the Maintenance Menu select Extended BIT Summary display.

ac. Verify the Extended BIT Summary display (figure 3-7) appears; after a predetermined amount of time (enough time to ensure all extended BIT routines have been run; as shown on Extended BIT Summary display), select Halt BIT.

ad. Select Tests 1-8 and verify the display changes to BIT Results display (figure 3-8).

ae. Verify all tests passed (view BIT Results screen 2 (figure 3-9) also; test 9) and all applicable LRUs show a good status.

af. Verify the MCP PWA RUN LED is turned on green.

ag. Verify the SYNTH PWA LOCK LED is turned on.

ah. Select previous menu until the Select Menu appears.

ai. Verify the front panel TEST indicator and the FAULT indicator are turned off and the NORMAL indicator is turned on.

aj. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

ak. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

al. Tighten four front-panel captive screws to the cabinet assembly.

am. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

an. Further IR operational verification is performed by utilizing the MTG. Refer to O&M manual applicable to suspect IR equipment group (see section 3, paragraph 3-11); otherwise, proceed with step ao.

ao. Place the REMOTE/LOCAL switch to the REMOTE position. Notify the TOCC2 operator that the IR is online and ADPE operation (remote control) is enabled.

5—7 Removal/Replacement

The following procedures provide removal and replacement instructions for IR major components. The procedures are presented in a step-by-step format to facilitate user comprehension and simplify task complexity. Tools or equipment required for removal and replacement of IR components are identified in the text, where applicable. These procedures assume that IR has been health tested in accordance with the procedures in paragraph 5-4 and that one or more LRUs have been identified as defective.

WARNING

Before attempting to perform any troubleshooting procedures, ensure that power has been removed (when possible) to prevent injury or DEATH from electric shock. It is recommended that at least two people are present at all times when working on energized equipment.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5—8 PWA Replacement

The IR PWAs are mounted in a card cage accessible from the top of the unit. The primary ac power must be turned off before replacing a PWA. When inserting PWAs, care must be used to ensure that connectors are properly aligned before applying engaging force. Perform the following procedure when a defective PWA is identified.

a. Set AC POWER ON/OFF switch to OFF

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Using a flat-tipped screwdriver, loosen four captive screws securing top cover to maintenance panel. Raise top cover to gain access to PWAs.

e. Disconnect tagged RF cables from suspect PWA by gently pulling snap-on connector from PWA RF receptacle.

f. Using a flat-tipped screwdriver, loosen two captive screws securing PWA to chassis.

g. Grasping both PWA handles, push outward, unseat and remove PWA.

NOTE

For the MCP PWA, SP7472100 - XXX IC chips (J21, J23, J25, and J27) and the DMDP PWA, SP7472110 - XXX IC chips (J11 and J12) must be removed from faulty PWA and inserted onto the new PWA. Perform the IC chip replacement paragraph 5 - 9 prior to installing the new MCP or DMDP PWAs.

Figure 5 - 3 shows the MCP PWA jumper locations. Refer to table 5 - 4 for jumper descriptions and settings. Also shown are the four EPROM socket locations for SP7472100 - XXX IC chip set and proper installation alignment. Figure 5 - 4 shows the DMDP PWA EPROM socket locations for SP7472110 - XXX IC chip set and proper installation alignment.

h. Install replacement PWA in its appropriate slot and apply pressure to ensure proper seating.

i. Using a flat-tipped screwdriver, secure PWA to chassis with captive screws.

j. Reconnect RF cables to replacement PWA by gently seating RF cable to PWA SMB connector.

k. Inspect unit to ensure proper reassembly.

l. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

m. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

n. Tighten four front-panel captive screws to the cabinet assembly.

o. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

p. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—9 IC Chip Replacement

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

a. Place faulty PWA on an ESD approved work bench.

b. For the MCP, refer to figure 5-3 and identify SP7472100-XXX IC chip set and chip key placement (J21, J23, J25, and J27). For the DMDP, refer to figure 5-4 and identify SP7472110-XXX IC chip set and chip key placement (J11 and J12).

c. Using a standard commercial IC chip puller, carefully extract IC chip set.

d. Place each chip in ESD approved conductive foam.

e. Package faulty PWA as per procedure in section 2; paragraph 2-7.

f. Place new PWA on ESD approved work bench.

g. Referring to applicable figure (5-3 or 5-4) re-insert IC chip set. Ensure chip key placement is correct.

h. Referring to figure 5-3 and table 5-4, verify/ ensure all MCP PWA jumper settings are correct.

i. Replace PWA per procedure in paragraph 5-8.

5—10 Cooling Fan Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat-tipped screwdriver, loosen four captive screws and eight quick-disconnect

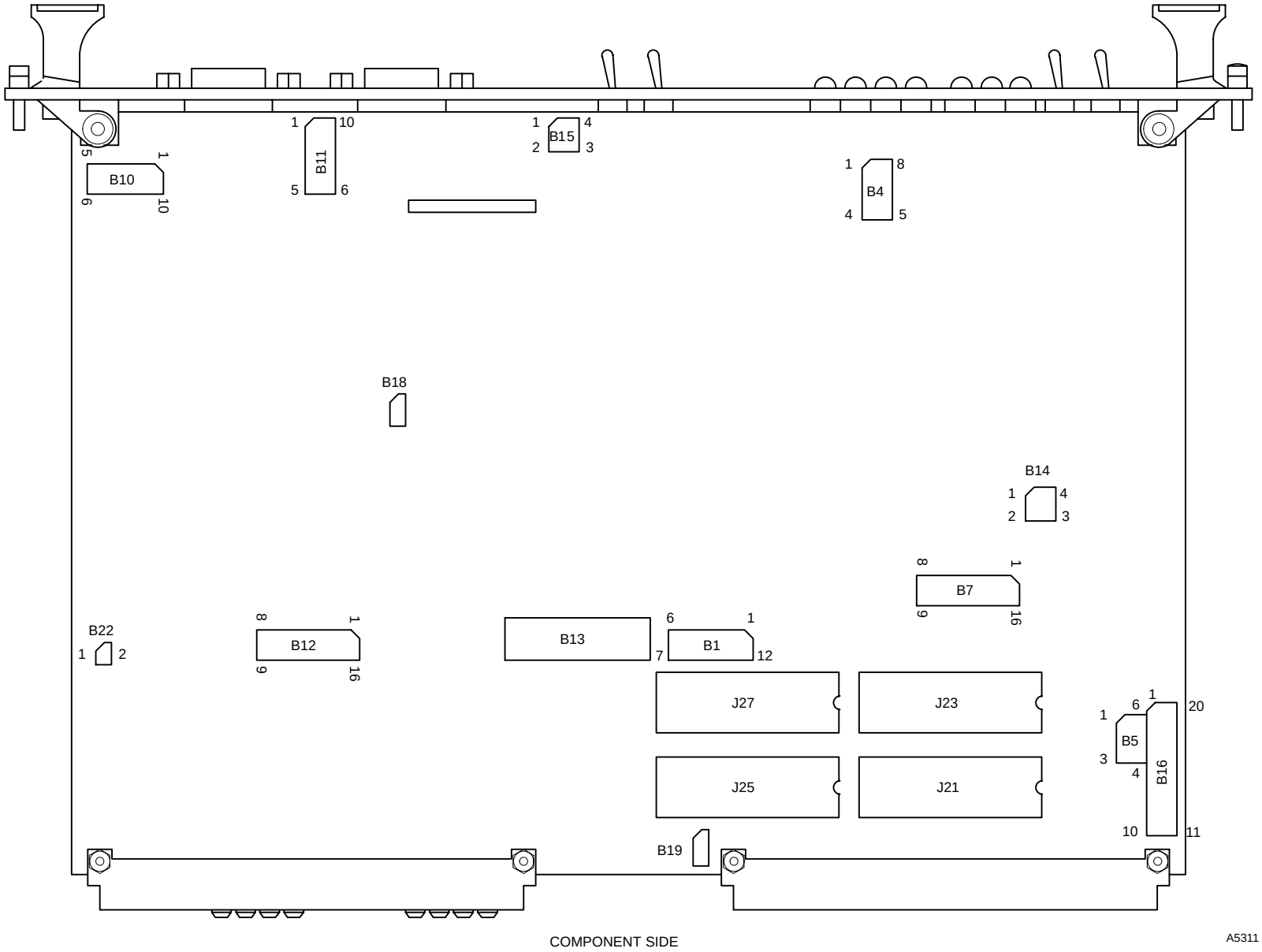


Figure 5—3. MCP PWA Component Location Diagram

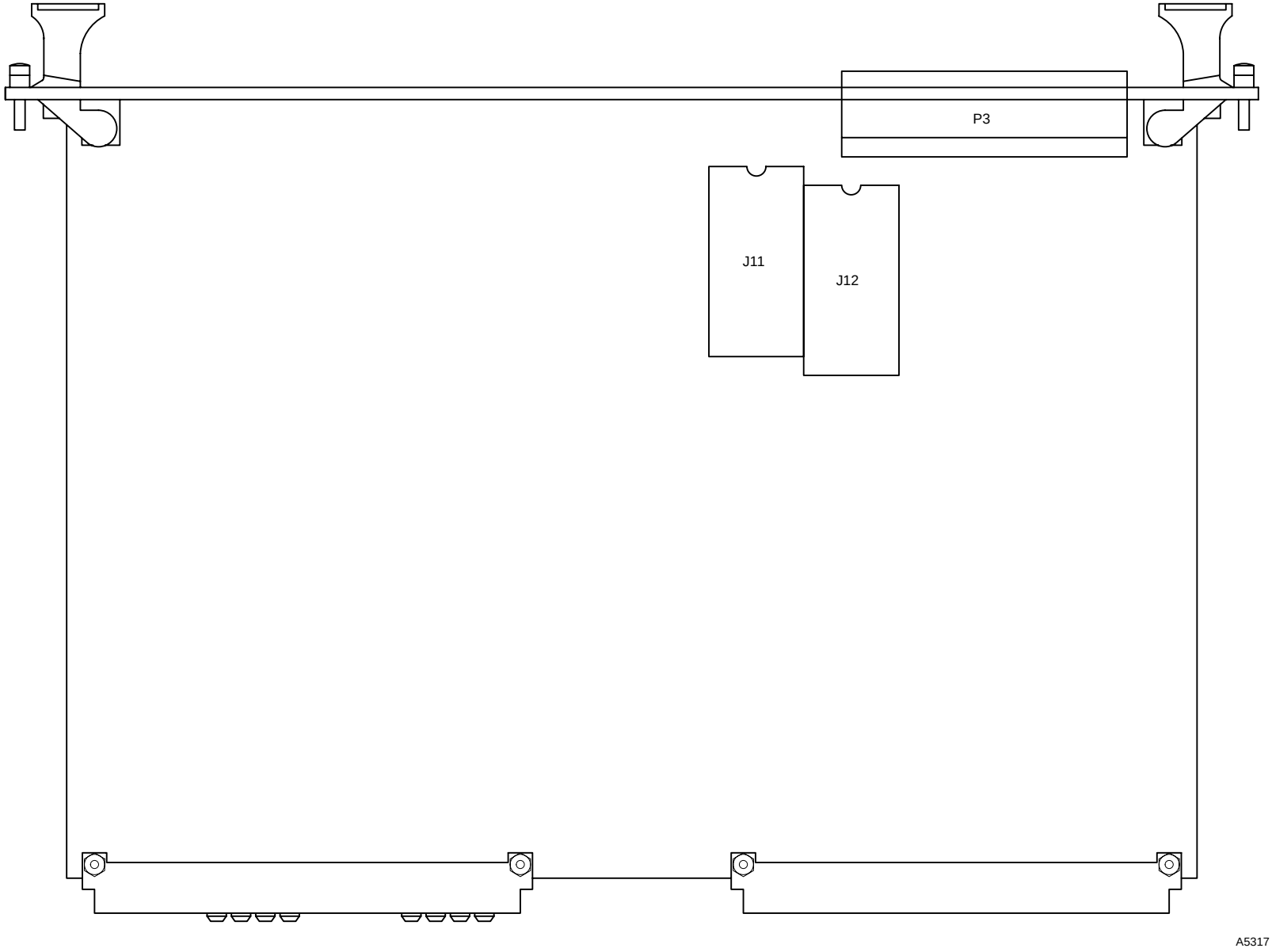


Figure 5—4. DMDP PWA Component Location Diagram

Table 5—4. MCP Jumper Configurations

JUMPER BLOCK	JUMPER BLOCK DESCRIPTION	JUMPERS INSTALLED	CONFIGURED JUMPER FUNCTION
B1	Address comparator for SRAM	1 - 12, 3 - 10, 5 - 6, 8 - 9	1 Mbyte local SRAM
B4	Access time selection for EPROM area	3 - 6, 4 - 5	200 ns EPROMs
B5	Clock to Bus Reset to Bus Reset from Bus	1 - 6, 2 - 5, 3 - 4	Clock enabled to bus Reset enabled to bus Reset enabled from bus
B7	EPROM area address decoding	1 - 16, 2 - 15, 3 - 14, 4 - 13	EPROM type: 27C010 Org: 512K x 8
B10	Serial interface MPCC1 RS232 control	2 - 3, 4 - 7, 5 - 6	DSR - DSR (out) DCD - CTS (in) DTR - DTR (out)
B11	Serial interface MPCC2 RS232 control RS422/485 control	2 - 3, 4 - 7, 5 - 6	- DSR - CTS - DTR
B12	VMEbus interrupts	1 - 16, 2 - 15, 3 - 14, 4 - 13, 5 - 12, 6 - 11, 8 - 9	IRQ1 thru IRQ6 enabled IRQ7 disabled VME PROM disabled
B13	User I/O, S/W readable	None	Not used
B14	Long time bus error enable	2 - 3	
B15	Threshold of the power voltage detector	1 - 4	4.65 to 4.70 volt threshold
B16	Serial interface MPCC2 RS232 control RS422/485 control	1 - 20, 3 - 18, 4 - 17, 5 - 6, 7 - 14, 11 - 12, 15 - 16	Bus request level 3
B18	Abort to IRQ7	None	Not used
B19	Power standby for the SRAM 4.5V minimum	None	Standby power disabled
B22	VSB enable/disable	1 - 2	VSB disabled

screws securing top cover and remove top cover.

f. Remove air filter at rear of unit by sliding filter upward.

g. Disconnect/tag ac power plug from suspect fan.

h. Using a flat-tipped screwdriver, remove four each flat-head screws, flat washers, and lock nuts retaining faulty fan.

i. Remove faulty fan and protective cover.

j. Mount replacement fan and previously removed protective cover by replacing four each flat-head screws, flat washers, and lock washers previously removed in step (h).

k. Reconnect air filter ac power plug and air filter.

l. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel and eight quick-disconnect screws to chassis.

m. Reconnect ac power cord to rear panel connector J101.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front-panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—11 PS1 and PS2 Replacement

NOTE

Before replacing suspect faulty power supply, attempt to correct power supply fault by toggling unit power to reset power supply circuit breaker and then perform the adjustment procedures in paragraph 5 - 3.

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

e. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

f. Carefully lower bottom panel to gain access to power supplies.

g. Tag all power lines connected to suspect power supply.

h. Disconnect power lines from power supply terminals using a flat-tipped screwdriver.

CAUTION

Secure power supply by applying pressure/firmly holding as mounting screws are removed. Failure to do so may result in damage to power supply due to slippage.

i. While applying pressure to power supply, use a No. 2 cross-tipped screwdriver to remove (four - PS2 or three - PS1) pan-head locking screws securing suspect power supply to bottom cover and store power supply in a secure area.

j. While firmly holding new power supply, use No. 2 cross-tipped screwdriver to replace (four - PS2 or three - PS1) pan-head locking screws removed in step (i) to secure power supply to bottom cover.

k. Reconnect power lines to their appropriate terminals using a flat-tipped screwdriver.

l. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

m. Reconnect ac power cord to rear panel connector J101.

n. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

o. Tighten four front-panel captive screws to the cabinet assembly.

p. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

q. Perform paragraph 5-3 before operating IR.

r. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—12 PS3 Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat-tipped screwdriver, loosen four captive screws securing top cover to maintenance panel and raise top cover.

f. Disconnect connector P6 from the maintenance panel connector J6. Remove A1J23 from A1 P23 with No. 1 standard screwdriver.

g. Using a No. 2 cross-tipped screwdriver, remove four pan-head screws securing maintenance panel to unit chassis.

h. Carefully lift maintenance panel and tag/disconnect RF cables from maintenance panel connectors J1 through J5. Flip backwards and carefully lay on card cage.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

i. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

j. Carefully lower bottom panel to gain access to terminal board 2 (TB2). Remove TB2's cover.

k. Using a flat-tipped screwdriver, disconnect the three ac power lines and 130 Vdc lines (log which wires attach to which TB2 terminals) from TB2 terminals which originate from PS3; then remove TB2.

l. While applying pressure to power supply, use a No. 2 cross-tipped screwdriver to remove 4 flat-head screws securing PS3 bracket to chassis side panel.

m. Using a No. 2 cross-tipped screwdriver, remove four flat-head screws securing power supply cover to chassis side panel and carefully store it in a secure area.

CAUTION

Secure power supply No. 3 by applying pressure/firmly holding as mounting screws are removed. Failure to do so may result in damage to power supply due to slippage.

n. Remove PS3 from unit and at workbench (when applicable), remove bracket assembly from defective PS3 and attach to new PS3. Store defective PS3 in a secure area.

o. While firmly holding new PS3 with bracket, use No. 2 cross-tipped screwdriver to replace two flat-head screws removed in step (m) to secure power supply to chassis side panel.

p. Reposition power supply cover over PS3 with power lines fed through feed-hole.

q. Using a No. 2 cross-tipped screwdriver, replace four flat-head screws securing power supply cover to chassis side panel.

r. Using a flat-tipped screwdriver, reconnect the three ac power lines and 130 Vdc lines to TB2 terminals (refer to log taken in step k).

s. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

t. Carefully lift maintenance panel and reconnect RF cables to maintenance panel connectors J1 through J5.

u. Carefully place maintenance panel into its correct position within the chassis and using a

No. 2 cross-tipped screwdriver, replace the four pan-head screws securing the maintenance panel to the chassis.

v. Reconnect connector P6 to the maintenance panel connector J6.

w. Inspect IR to ensure proper reassembly.

x. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

y. Reconnect ac power cord to rear panel connector J101.

z. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

aa. Tighten four front-panel captive screws to the cabinet assembly.

ab. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

ac. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—13 Touch Panel Display Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

e. Using a flat-tipped screwdriver, loosen four captive screws securing top cover to maintenance panel and raise top cover.

f. Disconnect connector P6 from the maintenance panel connector J6.

g. Using a No. 2 cross-tipped screwdriver, remove four pan-head screws securing maintenance panel to unit chassis.

h. Carefully lift maintenance panel and lay against card cage.

i. Using a No. 2 cross-tipped screwdriver, remove four pan-head screws securing touch panel screen assembly. Carefully remove screen assembly by prying assembly loose from guide pins on front panel assembly. Store screen assembly in a secure area.

CAUTION

Secure display panel by applying pressure/firmly holding as screws and connectors are removed. Failure to do so may result in damage to panel due to slippage.

j. While applying pressure to display panel, use a No. 2 cross-tipped screwdriver to remove four outer flat-head screws securing panel to unit front panel.

k. While firmly holding display panel, remove connectors (A7P3 and A7P4) to release panel from unit front panel.

l. While firmly holding display panel, use No. 2 cross-tipped screwdriver to remove four flat-head screws holding panel in its housing and remove panel from housing. Place defective display panel in a secure area.

Note

The infrared emitters and sensors associated with the display panel switch function are mounted on the electronic module. They fire toward the display viewer and depend upon prisms mounted along the bezel periphery to reflect the infrared beams parallel to the display surface. This scheme requires careful attention to display panel mounting. The under surface of the bezel must be held parallel to the top of each of the four spacers upon which the electronic module mounts to the rear of the unit front panel.

Prior to installing display panel to unit front panel, ensure that DIP switches 1, 2, and 3 located on the display control boards are set properly for the unit configuration (refer to figure 5-5). Compare with replaced display panel to ensure proper switch settings.

m. Install new display panel in housing.

n. While firmly holding display panel, use No. 2 cross-tipped screwdriver to replace four flat-head screws removed in step (l) to secure panel to housing (two longer screws go in top two positions).

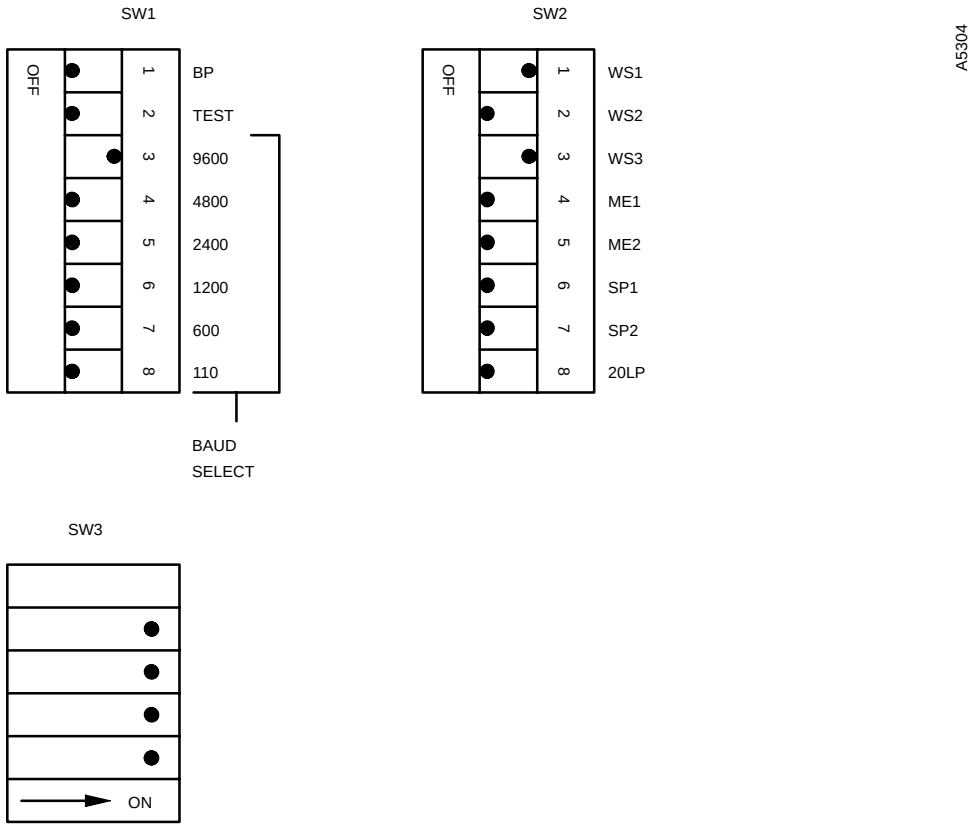


Figure 5—5. Touch Panel Display Dip Switch Settings

CAUTION

Secure display panel by applying pressure/firmly holding as screws and connectors are replaced. Failure to do so may result in damage to panel due to slippage.

o. While firmly holding display panel, replace connectors removed in step (k).

p. While applying pressure to display panel, secure panel to unit by using a No. 2 cross-tipped screwdriver to replace four flat-head screws removed in step (j).

q. Reinstall the black touch panel bezel by using a No. 2 cross-tipped screwdriver to replace the four pan-head screws removed in step (i).

r. Carefully lift maintenance panel and reconnect RF cables to maintenance panel connectors J1 through J5.

s. Carefully place maintenance panel into its correct position within the chassis and using a No. 2 cross-tipped screwdriver, replace the four pan-head screws securing the maintenance panel to the chassis.

t. Reconnect connector P6 to the maintenance panel connector J6, J23 to A1 P23.

u. Inspect IR to ensure proper reassembly.

v. Close top cover and using a flat-tipped screwdriver, tighten four top cover captive screws to maintenance panel.

w. Reconnect ac power cord to rear panel connector J101.

x. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

y. Tighten four front-panel captive screws to the cabinet assembly.

z. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

aa. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—14 Lamp Replacement

a. Grasp the lamp cover with the thumb and forefinger and remove it by unscrewing it from the lampholder assembly.

b. Grasp the lamp with the thumb and forefinger and remove it by pulling outward.

c. Reinsert replacement lamp; lamp is keyed so it will fit into lampholder only one way.

d. Replace lamp cover by screwing it back onto the lampholder; do not overtighten.

e. Verify proper operation of replacement lamp by running the confidence BIT.

f. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—15 Lampholder Replacement

a. Preheat a soldering iron.

b. Set AC POWER ON/OFF switch to OFF.

c. Loosen the four captive screws holding the unit in the cabinet.

d. Slide the unit forward until the rail guide locks are set to the locked position.

e. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

f. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

g. Carefully lower bottom panel to gain access to suspect lampholder.

h. Remove protective shrink wrap from lampholder connectors. Wrap may be removed by slipping it down the wire or by carefully cutting it off using a pair of snub-nosed wire cutters.

i. Tag lampholder wires connected to positive and negative leads.

j. Using preheated soldering iron, unsolder tagged wire connected to lampholder leads.

k. Using 1/2” open-end wrench, grasp mounting flange nut (on inside of front panel) holding lampholder to chassis. With free hand, grasp lampholder section on outside of front panel.

l. Unscrew flange nut and remove lampholder from chassis.

m. Replace new lampholder into front panel and screw flange nut finger tight onto chassis.

n. Using 1/2” open-end wrench, grasp mounting flange nut (on inside of front panel) holding lampholder to chassis. With free hand, grasp lampholder section on outside of front panel.

o. Tighten flange nut to ensure a firm mounting to chassis.

p. Place or ensure that an ample amount of shrink wrap is resident on each wire prior to soldering.

q. Using the preheated soldering iron, solder previously removed wires to respective positive and negative lampholder leads.

r. Shift the shrink wrap so it covers the new soldered joint.

s. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

t. Reconnect ac power cord to rear panel connector J101.

u. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

v. Tighten four front-panel captive screws to the cabinet assembly.

w. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

x. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—16 Switches and Circuit Breaker Replacement

a. Set AC POWER ON/OFF switch to OFF.

b. Loosen the four captive screws holding the unit in the cabinet.

c. Slide the unit forward until the rail guide locks are set to the locked position.

d. Disconnect ac power cord from rear panel connector J101.

CAUTION

Secure bottom cover by applying pressure as mounting screws are loosened. Failure to do so may result in damage to unit.

e. Applying pressure to bottom cover towards unit chassis, use a flat-tipped screwdriver to loosen nine captive screws securing bottom cover to unit chassis.

f. Carefully lower bottom panel to gain access to switches and circuit breaker.

g. Tag all wires connected to suspect switch or circuit breaker, after removing heatshrink that surrounds switch or circuit breaker.

h. Using the appropriate flat-tipped or cross-tipped screwdriver, disconnect wire leads connected to suspect switch or circuit breaker.

i. Using 9/16″ open-end wrench, grasp mounting flange nut (on outside of panel) holding suspect switch or circuit breaker to chassis. With free hand, grasp section on inside of panel.

j. Unscrew flange nut and remove from chassis.

k. Replace new switch or circuit breaker into panel and screw flange nut finger tight onto chassis.

l. Using 9/16″ open-end wrench, grasp mounting flange nut (on outside of panel) holding switch or circuit breaker to chassis. With free hand, grasp section on inside of panel.

m. Tighten flange nut to ensure a firm mounting to chassis.

n. Place ample amount of heatshrink on switch.

o. Using appropriate flat-tipped or cross-tipped screwdriver, re-connect wire leads to new switch or circuit breaker.

p. Using a heat blower gun, form heatshrink over switch to adequately cover power leads.

q. Carefully raise bottom cover and using a flat tipped screwdriver, tighten nine captive screws securing bottom cover to unit chassis.

r. Reconnect ac power cord to rear panel connector J101.

s. Disengage the rail guide locks and slide unit slowly into equipment cabinet ensuring a clear entry.

t. Tighten four front-panel captive screws to the cabinet assembly.

u. Make a visual inspection ensuring no cables are being pinched and that the unit is properly seated within the cabinet assembly.

v. Perform paragraph 5-6 Operational Verification to verify IR operability.

5—17 Preventive Maintenance

Preventive maintenance serves to keep the equipment in proper operating condition, to prevent breakdown, and to hold needless repair to a minimum. This information includes cleaning equipment required and instructions for preventive maintenance. As a general rule, the preventive maintenance measures detailed in the following paragraphs should be accomplished once a month or per site requirements. When the unit is operated under severe contamination conditions (for example, dust or dirt) a shorter preventive maintenance interval is recommended. Turn off or disconnect the input power before performing the preventive maintenance procedures.

WARNING

Before attempting to perform inspection or preventive maintenance, ensure that power has been removed to prevent injury or DEATH from electric shock.

CAUTION

This equipment contains parts sensitive to damage by electrostatic discharge (ESD). Use ESD Class 1 precautionary procedures when touching, removing, or inserting parts or assemblies.

5—18 Inspection

Visual inspection of the unit should be performed once every 30 days or per site requirements. Visually inspect the unit to determine if the item is damaged or incomplete to the extent that it should be repaired or replaced. Perform the visual inspection procedures in table 5-5.

5—19 Preventive Maintenance Steps

Preventive maintenance consists of inspection, cleaning, and voltage checks. The unit should be cleaned every 30 days or per site requirements. Clean exterior surfaces using a clean lint-free cloth to remove dust or grease. Perform interior preventive maintenance as follows:

a. Using a vacuum cleaner, remove loose dust and dirt from card cage, PWAs, and interior surface.

b. Use a soft-bristle brush to remove dirt that adheres to the card cage, PWAs, and interior surfaces.

c. Remove air filter from behind 3-form frame, clean using a vacuum cleaner or reverse flushing with water, and replace air filter when dry.

d. Verify fan (3) rotation is free of restriction. Clean fan blades of dust accumulation.

e. Using a digital voltmeter, verify power supply voltages (via the maintenance panel test points) are within specification. Refer to paragraph 5-3 if adjustments are necessary.

Table 5—5. Inspection and Maintenance Criteria

ITEM	NOMENCLATURE	INSPECT FOR	REPAIR
1	Exterior	Dents, scratches, loose cable connectors, paint damage	Repair or replace
2	Interior	Dents, scratches, loose cable connectors, broken wires, evidence of burned or charred components, defective solder connections	Repair or replace

Section 6 — Parts List

6—1 Introduction

This section lists, describes, and illustrates a breakdown of items necessary to support the Integrated Receiver. The purpose of the breakdown is to assist supply and maintenance personnel in identifying, requesting, and stockpiling IR replacement parts.

6—2 List of Manufacturers

Table 6-2 contains the list of manufacturer commercial and government entity (CAGE) numbers/federal supply code for manufacturers (FSCM), names, and addresses for all items listed in the parts lists.

6—3 Maintenance Parts List

The maintenance parts lists (MPLs) (refer to table 6-1 for a list of MPLs, tables 6-3 through 6-6) provide a description of each major assembly, subassembly, and attaching part listed, keyed to the applicable figure (e.g., figure 6-2, index 4 is identified in the first column of the corresponding MPL as 6-2-4). Other information in the MPLs include item reference designator, item nomenclature/description, manufacturer's code (CAGE/FSCM), item part number, and number of units per assembly. These items are all described in the following paragraphs.

6—4 Reference Designator Column

The reference designator allows for an indexed item designation reference to the top assembly.

6—5 Figure and Index Number Column

This column lists the applicable index numbers called out on the associated figure.

6—6 Description Column

This column contains the nomenclature and description of each assembly, subassembly, or attaching part. Subassemblies within an assembly are indented under that assembly with individual index numbers assigned to them. Attaching parts hardware is indented under the item it attaches, and the description is followed by the attaching part annotation "(AP)."

6—7 CAGE/FSCM Column

This column provides the parts manufacturers' CAGE/FSCM codes. These codes relate to the manufacturers listed in table 6-2 and are in accordance with Federal Supply Codes for Manufacturers Cataloging books H4-1, H4-2, and H4-3.

6—8 Part Number Column

This column contains the manufacturer's part number for the indexed part in the associated figure. A number sign (#) following the part number indicates that the item is either government-furnished equipment (GFE), contractor-furnished equipment (CFE), or attachment hardware covered in other manuals.

6—9 Quantity Column

This column indicates the quantity required for an assembly, subassembly, or piece part. If quantities are indefinite (i.e., adhesive, locktite, etc.), an "AR" is placed in this column to indicate "as required." If the quantity of the item has been called out in a previous figure or if the item must be removed to gain access to a spared item, a "REF" is placed in this column to indicate "reference".

6—10 Illustrations

Figures 6-1 through 6-4 (refer to table 6-1 for a list of parts illustrations) are illustrated parts breakdowns (IPBs) showing the major assemblies, subassemblies, and attaching parts associated with the IR. Individual items in each figure are identified with an index number and keyed to the corresponding MPL, which normally faces and immediately follows the figure.

Table 6—1. List of Parts Lists and Figures

Table 6—2. Index to Manufacturers CAGE/FSCM Numbers		
CAGE/ FSCM	MANUFACTURER	ADDRESS
03102	Supreme Supply Co.	734 E. Hyde Park Blvd. P.O. Box 922 Inglewood, CA 90302-2508
05236	Jonathan Mfg. Co.	Fullerton, CA
07421	Interstate Electronics Corp.	1001 E. Ball Road P.O. Box 3117 Anaheim, CA 92803
08742	Emerson Electric Co. ACDC Electrics Div.	401 Jones Rd. Oceanside, CA 92054-1216
09353	C and K Components Inc.	15 Riverdale Ave. Newton, MA 02158-1057
25140	Globe Motors	2275 Stanley Ave. Dayton, Ohio 45404
27193	Eaton Corp. Aerospace/Commercial	Controls Div. Milwaukee, WI
28979	Wavecom	9036 Winnetka Ave. Northridge, CA 91324-3235
72619	Dialight Corp. Brooklyn Div.	203 Harrison Pl. Brooklyn, New York 11237-1587
80103	VEECO Instruments Inc. Lambda Electronics Div.	515 Broad Hollow Rd. Melville, New York 11747-3703
80205	National Aerospace Standards Committee Aerospace Industries Association of America, Washington, DC. Sources of supply for all of the National Aerospace Standards have been identified and compiled into a reference book published by the National Standards Association. This book is available through Federal Supply Schedule 76, Part I.	
81349	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3-M.	
8Z410	Ledtronics Inc.	Harbor City, CA
96906	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3-M.	
NMB	NMB Technologies Inc. Motor Division	Chatsworth, CA

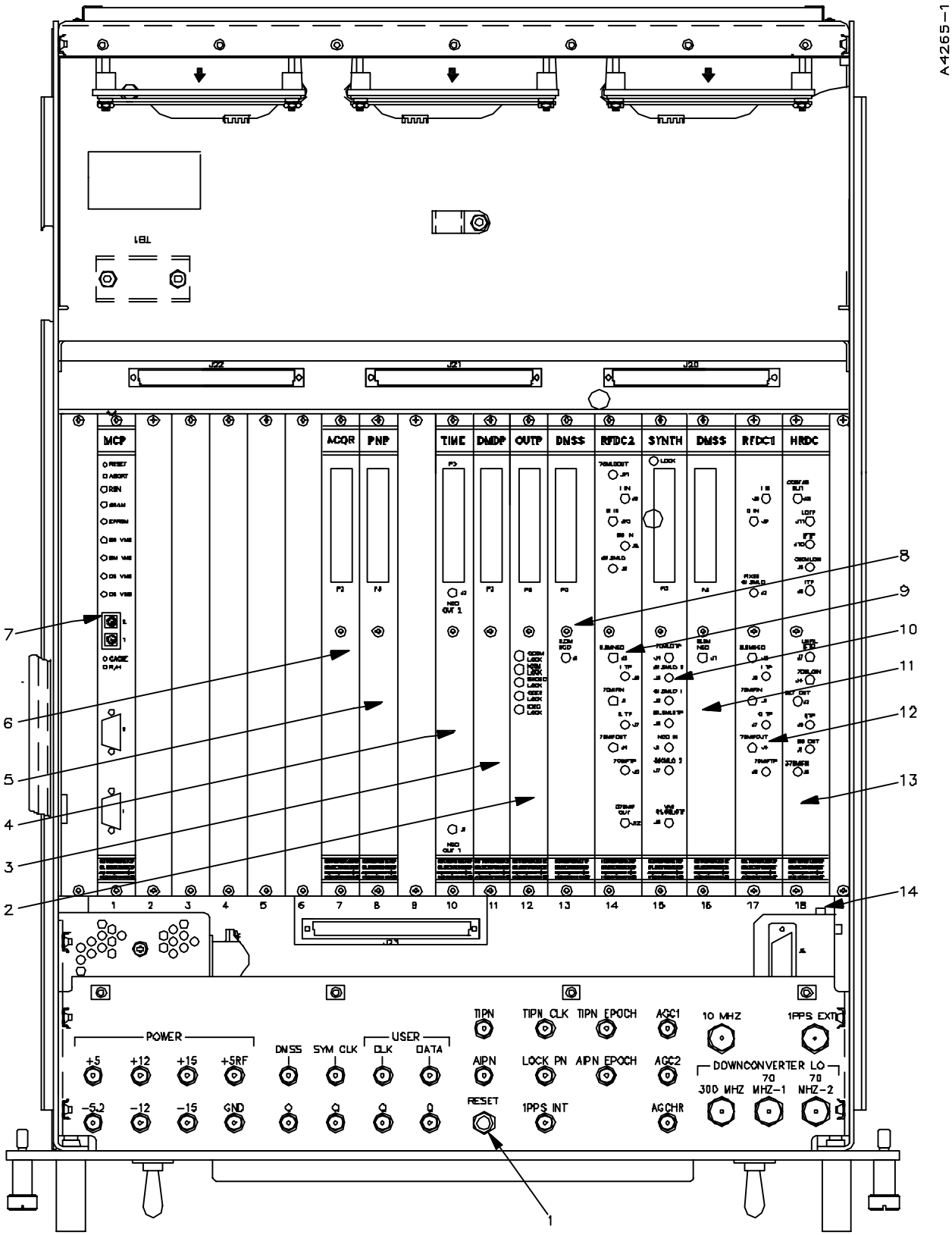


Figure 6—1. Integrated Receiver (Top View)

Table 6—3. Parts List, Integrated Receiver (Top View)

REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6-1	Integrated Receiver (Top View)	07421	7472100	REF
1A6SW4	6-1-1	. Switch, Push . . Cap, Nylon (AP)	09353 09353	8121ZE 7527-2	1 1
1A4A12	6-1-2	. Output Processor PWA	07421	7473400-502	1
1A4A11	6-1-3	. Demod Processor PWA . . Firmware Chip Set (J11 and J12) (AP)	07421 07421	7476100 SP7472110-XXX*	1 1
1A4A10	6-1-4	. Timing Generator PWA	07421	7473000-502	1
1A4A8	6-1-5	. PN Processor PWA	07421	7473300-501	1
1A4A7	6-1-6	. Acquistion Processor PWA	07421	7473200-501	1
1A4A1	6-1-7	. Modem Control Processor PWA . . Firmware Chip Set (J21, J23, J25, and J27) (AP)	07421 07421	7473600 SP7472100-XXX*	1 1
1A4A13	6-1-8	. Demodulator Symbol Synchronizer PWA	07421	7473100-502	1
1A4A14	6-1-9	. RF Downconverter No. 2 PWA	07421	7474300-500	1
1A4A15	6-1-10	. Synthesizer PWA	07421	7474600-500	1
1A4A16	6-1-11	. Demodulator Symbol Synchronizer PWA	07421	7473100-502	1
1A4A17	6-1-12	. RF Downconverter No. 1 PWA	07421	7474000-500	1
1A4A18	6-1-13	. High Rate Downconverter PWA (KSA configuration only)	07421	7510500	1
1A6SW3, SW4	6-1-14	. Switch, RF Coaxial	28979	8021-A35-A4B-1CO	2

Note: *(XXX) represents the current firmware version.
Refer to figures 5-3 and 5-4 for chip location/placement.

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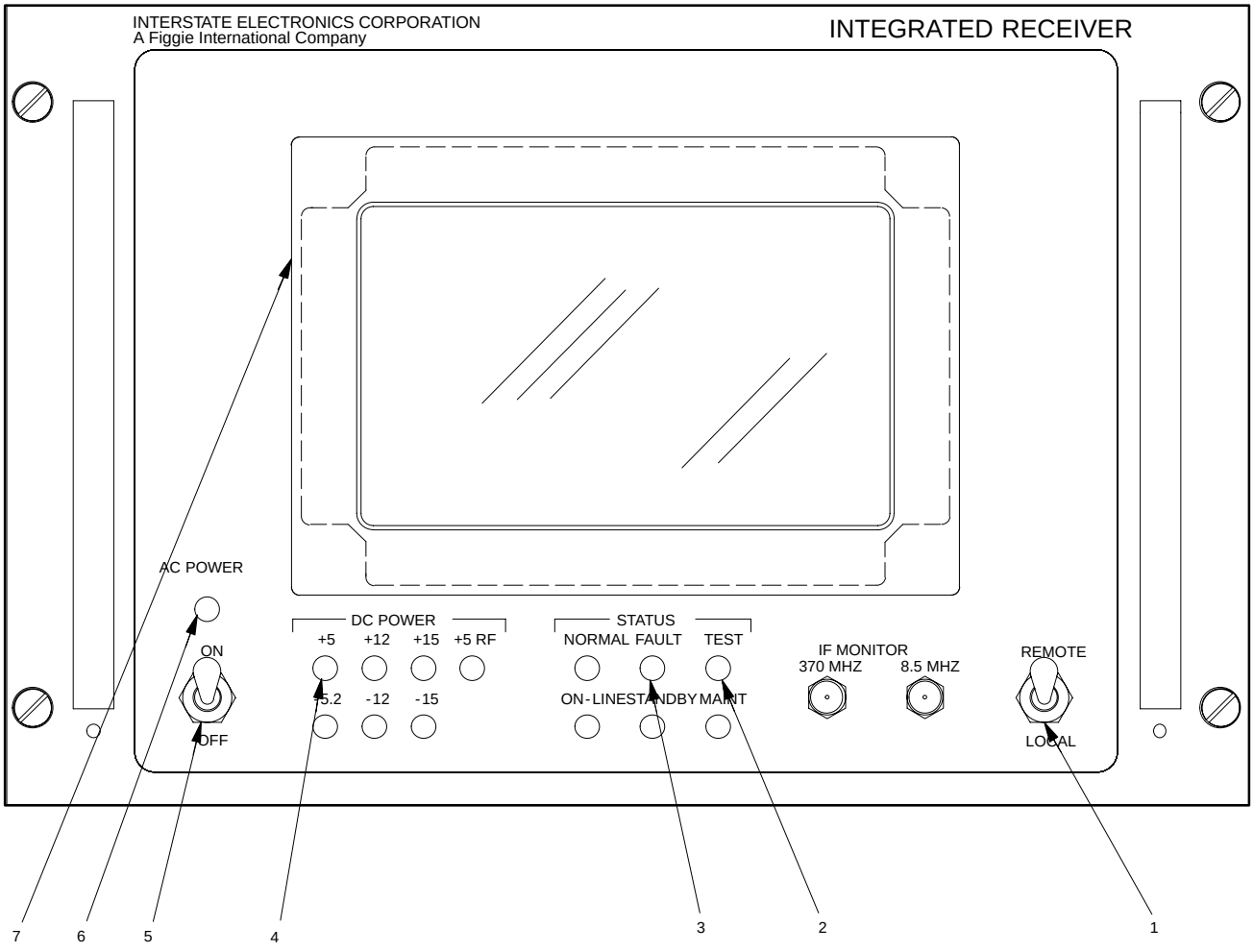

Figure 6—2. Integrated Receiver (Front View)

Table 6—4. Parts List, Integrated Receiver (Front View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6-2	Integrated Receiver (Front View)	07421	7472100	REF
1A7SW2	6-2-1	. Switch, Toggle	96906	MS24658-23F	1
1A7DS8	6-2-2	. Lamp, Cartridge . . Lampholder	72619 8Z410	507-4957-3733-500 DH0-30Y-D86BWC	1 1
1A7DS7	6-2-3	. Lamp, Cartridge . . Lampholder	72619 8Z410	507-4757-3731-500 DH0-30Y-D86BWC	1 1
1A7DS2-DS6, DS9-DS14	6-2-4	. Lamp, Cartridge . . Lampholder	72619 8Z410	507-4857-3732-500 DH0-30Y-D86BWC	11 11
1A7SW1	6-2-5	. Switch	81349	MS24659-22F	1
1A7DS1	6-2-6	. Lamp (LED), Cartridge	8Z410	CF296CWPG6-120VAC-R	1
1A7A1	6-2-7	. Touch Panel Display	07421	7519500	1

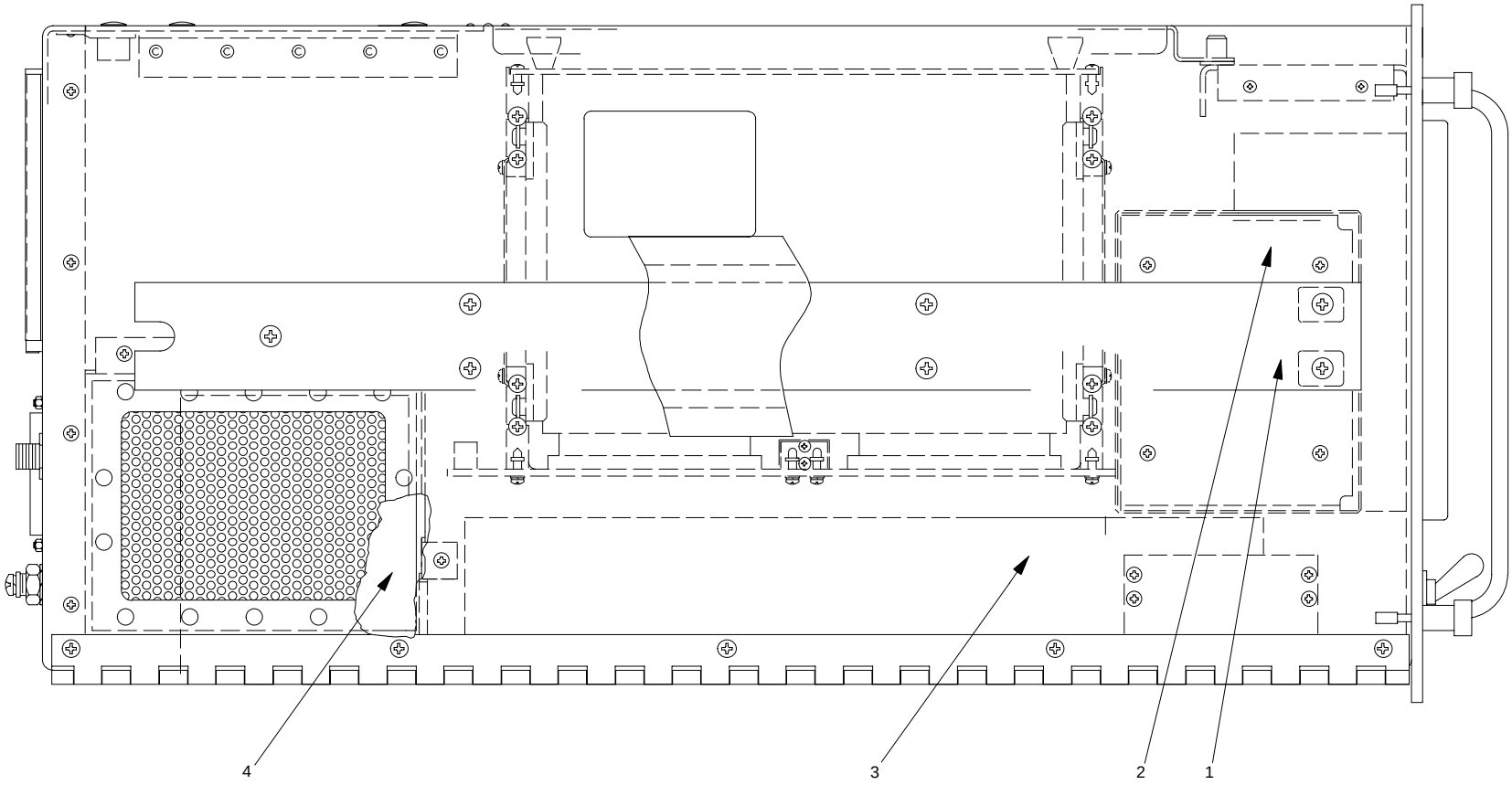

Figure 6—3. Integrated Receiver (Side View)

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Table 6—5. Parts List, Integrated Receiver (Side View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6-3	Integrated Receiver (Side View)	07421	7472100	REF
	6-3-1	. Slide, Section (Left)	05236	1505772B-L	1
	(Not Shown)	. . Screw, Cres FLH100 10-32X5/8 (AP)	96906	MS24693-C273	7
	6-3-1	. Slide, Section (Right)	05236	1505772B-R	1
		. . Screw, Cres FLH100 10-32X5/8 (AP)	96906	MS24693-C273	7
1A5	6-3-2	. Power Supply No. 3	07421	7516900	1
		. . Screw, FLH100 6-32X7/16 (AP)	96906	MS24693-C27	4
1A3	6-3-3	. Power Supply No. 2	08742	RMV223B-2330-0450	1
		. . Screw, PNH-LKG (AP)	80205	NAS1635-08LL8	4
		. . Washer (AP)	80205	MS15795-807	4
1A2	6-3-4	. Power Supply No. 1	80103	LFQ-27-1	1
		. . Screw, PNH-LKG (AP)	80205	NAS1635-08LL8	3
		. . Washer (AP)	80205	MS15795-807	3

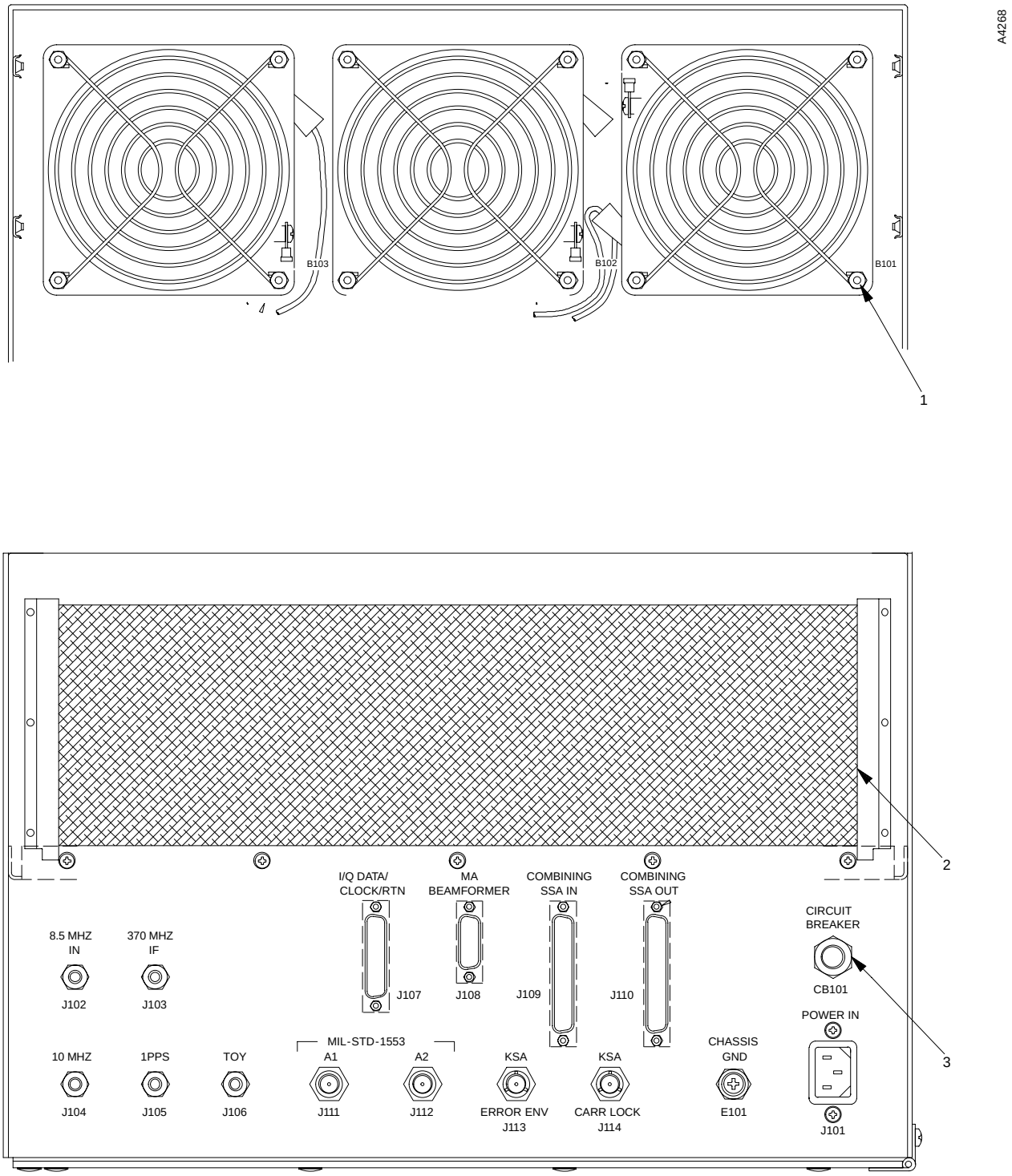

Figure 6—4. Integrated Receiver (Rear View)

Table 6—6. Parts List, Integrated Receiver (Rear View)					
REF. DES.	FIGURE/ IND. NO.	DESCRIPTION	CAGE/ FSCM	PART NUMBER	QTY
1	6-4	Integrated Receiver (Rear View)	07421	7472100	REF
1A1B101	6-4-1	. Fan, Tubeaxial	25140	A47-B15A-15T3-000	3
-B103		. . Grille, Metal (AP)	NMB	055015	3
		. . Screw, FLH 100 6-32X7/16 (AP)	96906	MS24693-C40	4
		. . Washer (AP)	96906	MS15795-805	4
		. . Nut (AP)	96906	MS21045C06	4
	6-4-2	. Filter, Air Cond	03102	3994-A	1
1A1CB101	6-4-3	. Circuit Breaker	81349	MS25244-10	1

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Section 7 — Drawings

7—1 Introduction

This section refers to drawings necessary for maintenance technicians to understand the makeup and function of the power, control, and signal inputs/outputs to and from the IR major components and subcomponents. These drawings allow the technicians to trace the path of each input/output, make continuity checks, perform general and specific trouble analysis of inoperative or malfunctioning IR functions, and locate components within the IR. Refer to table 7-1 for a list of drawings necessary for Level 1 maintenance.

Table 7—1. List of Drawings

FIGURE NUMBER	TITLE	DRAWING NUMBER
	Integrated Receiver Schematic Logic Diagram	EL7472101

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Glossary

The following defines the abbreviations, acronyms, and mnemonics used in this manual.

ACQR	Acquisition processor PWA
ADPE	Automated data processing equipment
AGC	Automatic gain control
ASIC	Application-specific integrated circuit
AP	Attaching part
AR	As required
A/D	Analog to digital
BB	Baseband
BCD	Binary-coded decimal
BER	Bit error rate
BERT	Bit error rate tester
BIM	Bus interrupter module
BIT	Built-in test
BITE	BIT equipment
BPF	Band-pass filter
BPSK	Binary PSK
CAGE	Commercial and government entity
CC	Common carrier
Comcor2	2-bit fast acquisition correlator chip
COTS	Commercial off-the-shelf
CPU	Central processing unit
CTFS	Common time and frequency system
CW	Continuous wave
C/No	Carrier-to-noise-density ratio
DAC	Digital-to-analog converter
dB	Decibel
dBm	Decibel unit of power level with reference to a power of one milliwatt
DMDP	Demodulator processor PWA
DMSS	Demodulator/symbol synchronization PWA
DoD	Department of Defense
DPRAM	Dual ported RAM
DSP	Digital signal processor
D/A	Digital to analog
Eb/No	Bit energy-to-noise ratio
ECL	Emitter coupled logic
EIRP	Effective isotropic radiated power
EMI	Electromagnetic interference
EPROM	Electrically programmable ROM
ESD	Electrostatic discharge
Exec	Executive program
FDU	Functional design unit
FFT	Fast fourier transform
FIR	Finite impulse response
FPCP	Floating-point coprocessor
FSCM	Federal supply code for manufacturers
GN	Ground network
GT	Ground terminal
HDR	High data rate
HMD	Hardware maintenance depot
HWCI	Hardware configuration item
I	Inphase
IC	Integrated Circuit
IEC	Interstate Electronics Corporation
IF	Intermediate frequency
IPB	Illustrated parts breakdown
IR	Integrated receiver
IRIG	Inter-range instrumentation group
ISR	Interrupt service routine
I/D	Integrate/dump
I/O	Input/output
kbps	kilobits per second
KSA	K-band single access
KSH	K-band shuttle
KSHR	K-band shuttle return service
LBI	Local bus interface
LDR	Low data rate
LMT	Line maintenance technician
LO	Local oscillator
LPF	Lowpass filter
LRU	Line replaceable unit
LSB	Least significant bit
MA	Multiple access
Mbps	Megabits per second
MCP	Modem control processor PWA
MDP	Modulator/Doppler Predictor
MHz	Megahertz
MIPS	Megainstructions per second
Mmax	Maximum-time-to-repair
MPPC	Multiprotocol communications controller

MPL	Maintenance parts list
MSB	Most significant bit
MTG	Maintenance test group
MTTR	Mean-time-to-repair
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NASCOM	NASA communications network
NCO	Numerically controlled oscillator
NGT	NASA ground terminal
NRZ-L	Non-return to zero-level
NRZ-M	Non-return to zero-mark
NRZ-S	Non-return to zero-space
O&M	Operation and maintenance
OUTP	Output processor PWA
PE	Probability of error
PI/T	Parallel interface and timer
PLL	Phased-lock loop
PMMS	Performance measuring and monitoring system
PN	Pseudorandom-noise
PNP	PN processor PWA
PS	Power supply
PSK	Phase-shift keying
PTE	PMMS test equipment
p-p	Peak-to-peak
QPSK	Quadrature PSK
RAM	Random access memory
RF	Radio frequency
RFDC	RF Downconverter PWA
ROM	Read-only memory
RTA	Remote terminal address
RTC	Real-time clock
R/H	Run/halt
R/R	Removal/replacement
SN	Space network
SNR	Signal-to-noise ratio
SPS	Symbols per second
SQPSK	Staggered QPSK
SRAM	Static RAM
SSA	S-band single access
SSH	S-band shuttle
SSHR	S-band shuttle return service
STDN	Spaceflight Tracking and Data Network
STGT	Second TDRSS Ground Terminal
	Tracking and Data Relay Satellite System
SYNTH	Synthesizer PWA
TB T	erminal board
TDRSS	Tracking and data relay satellite system
TIME	Timing generator PWA
TMS	Texas Instruments TMS320C25 DSP
TN	TDRSS network
TOCC2	TDRS Operations Control Center No. 2
TOY	Time-of-year
TS	Tri-state
TTL	Transistor-transistor logic
UQPSK	Unbalanced QPSK
USAT	User satellite
USS	User services subsystem
Vac	Voltage alternating current
VCO	Voltage controlled oscillator
VCXO	Voltage controlled crystal oscillator
Vdc	Voltage direct current
VME	Versa-Module European
VRTX	Versatile Real Time Executive